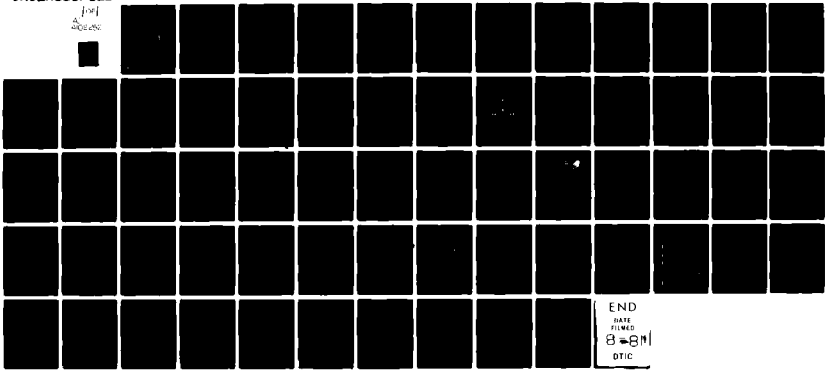
AD-A102 252 HUGHES RESEARCH LABS MALIBU CA F/G 9/2
HIGH-SPEED GAAS MESFET MEMORY STUDY.(U)
JUL 81 M WALDNER, R E LUNDGREN N00173-79-C-0191
UNCLASSIFIED NL



END
DATE FILMED
8-81
DTIC

12

HIGH-SPEED GaAs MESFET MEMORY STUDY

M. Waldner and R. E. Lundgren

Hughes Research Laboratories
3011 Malibu Canyon Road
Malibu, CA 90265

July 1981

N00173–79–C–0191
Final Report
For period 12 June 1979 to 11 September 1980

Approved for public release; distribution unlimited.

Prepared for
NAVAL RESEARCH LABORATORY
Washington, D.C. 20375

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

REPORT DOCUMENTATION PAGE

READ INSTRUCTIONS BEFORE COMPLETING FORM

1. REPORT NUMBER	2. GOVT ACCESSION NO. AD-A102252
3. RECIPIENT'S CATALOG NUMBER	
4. TITLE (and Subtitle) HIGH-SPEED GaAs MESFET MEMORY STUDY	5. TYPE OF REPORT & PERIOD COVERED Final Report 12 Jun 1979-11 Sep 1980
	6. PERFORMING ORG. REPORT NUMBER
7. AUTHOR(s) M. Waldner and R.E. Lundgren	8. CONTRACT OR GRANT NUMBER(s) N00173-79-C-0191
9. PERFORMING ORGANIZATION NAME AND ADDRESS Hughes Research Laboratories 3011 Malibu Canyon Road Malibu, CA 90265	10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS 61102F
11. CONTROLLING OFFICE NAME AND ADDRESS Naval Research Laboratory Washington, DC 20375	12. REPORT DATE July 1981
	13. NUMBER OF PAGES 65
14. MONITORING AGENCY NAME & ADDRESS(if different from Controlling Office)	15. SECURITY CLASS. (of this report) UNCLASSIFIED
	15a. DECLASSIFICATION DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited.

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18. SUPPLEMENTARY NOTES

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Semiconductor Memory
Random Access Memory (RAM)
GaAs Integrated Circuits (ICs)
GaAs MESFET
Enhancement-Mode MESFET

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

A design and analysis study of potential high-speed GaAs-MESFET memory circuits was performed. The results show that a 1-kbit static RAM having a 1-nsec access time is feasible. The design of the flip-flop memory cell uses low-power enhancement-mode MESFETs; power dissipation would be 5 μW per cell. To achieve maximum memory speed, the peripheral control and drive circuitry uses depletion-mode devices; total power

DD FORM 1 JAN 73 1473 EDITION OF 1 NOV 65 IS OBSOLETE

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

dissipation would be about 1 W. Experimental testing and characterization of the memory circuit designs will be performed during the second phase of the program.

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

SECTION 1

INTRODUCTION

The military has vital requirements for increasing the signal processing speed of integrated electronic systems for communication, radar, and electronic warfare. During the last several years, significant progress has been made in developing GaAs MESFET digital ICs operating in the 1 GHz to 5 GHz range. To fully exploit the potential applications of these fast logic circuits, it will also be necessary to have fast memory circuits with access times of 1 nanosecond, or less: high-speed buffer memories will be needed as interfaces between high-speed and slower-speed circuits, and fast cache or scratch-pad memories will be needed in high-speed signal processors for program and data storage. Ideally, the access and cycle times of these memories will be compatible with the fastest circuits with which they interact.

The goal of this program is to investigate the various device, circuit, and fabrication issues that are relevant to the development of high-speed GaAs random-access memories (RAMs): in particular, a 1-kbit static RAM with a 1-nsec access time. This report covers the first 15 months of this investigation.

A. APPROACH

In general, the highest GaAs operating speeds and drive currents are achieved with depletion-mode MESFETs (DFETs), but these devices are not suited for high-density LSI/VLSI applications because of high power dissipation. In contrast, the lowest power consumption and simplest circuitry are achieved with enhancement-mode MESFETs (ENFETs), which makes them attractive candidates for the realization of complex GaAs chips. ENFET circuits are normally slower than DFET circuits, however. Successful development of a nanosecond GaAs memory will require an optimum mix of both high-speed and low-power device properties. Therefore, our baseline approach is to use ENFETs to implement the necessary arrays of compact, low-power memory cells, and to use DFETs in the peripheral memory control and drive circuitry to achieve maximum speed. The results of the design analyses performed during the first year of this program support this approach.

The general organization of a 1-kbit static RAM that we have assumed for this study is described in part B of this first section. This organization was derived from that used in a 4-nsec bipolar memory developed by Hughes Radar Systems Group for the Ballistic Missile Defense Systems Command. Selection of the memory cell design is discussed in Section 2. ENFET inverters are used to implement a static flip-flop circuit, and access to the cell is controlled by DFET switches. Standby power dissipation is only 5 μW per cell. SPICE2 simulations were used to design and analyze the cell, the read sense amplifier, and the write driver. The design and analysis of the other major circuits (i.e., I/O latches, address decoders, and line drivers) are described in Section 3. The results of transient response-time analyses and power analyses are summarized in Section 4. Experimental verification is needed for all of the proposed circuit designs, thus Section 5 describes a memory test chip that will be fabricated and used to measure the dc and transient characteristics of the major memory circuits during the second year of the program.

B. RAM ORGANIZATION

Figure 1-1 shows a 1-K static RAM organized as 4 x 256 bits. This organization is optional and could be changed (e.g., to a 1 x 1024 arrangement) by additional decoding in the address lines to provide a block-select signal. The key point is that our analysis indicates that a 256-bit array of GaAs ENFET memory cells is compatible with the read and write-reset times required in a 1-nsec access memory.

The main features of the proposed memory organization are:

- The incorporation of data latches on the address inputs and on the input and output data lines.
- The provision of synch-enable logic, which allows the latching of prior output data in synchronism with the input of new address information. With synch-enable applied, the memory can operate in a pipeline mode; without it, it can operate in a conventional mode.

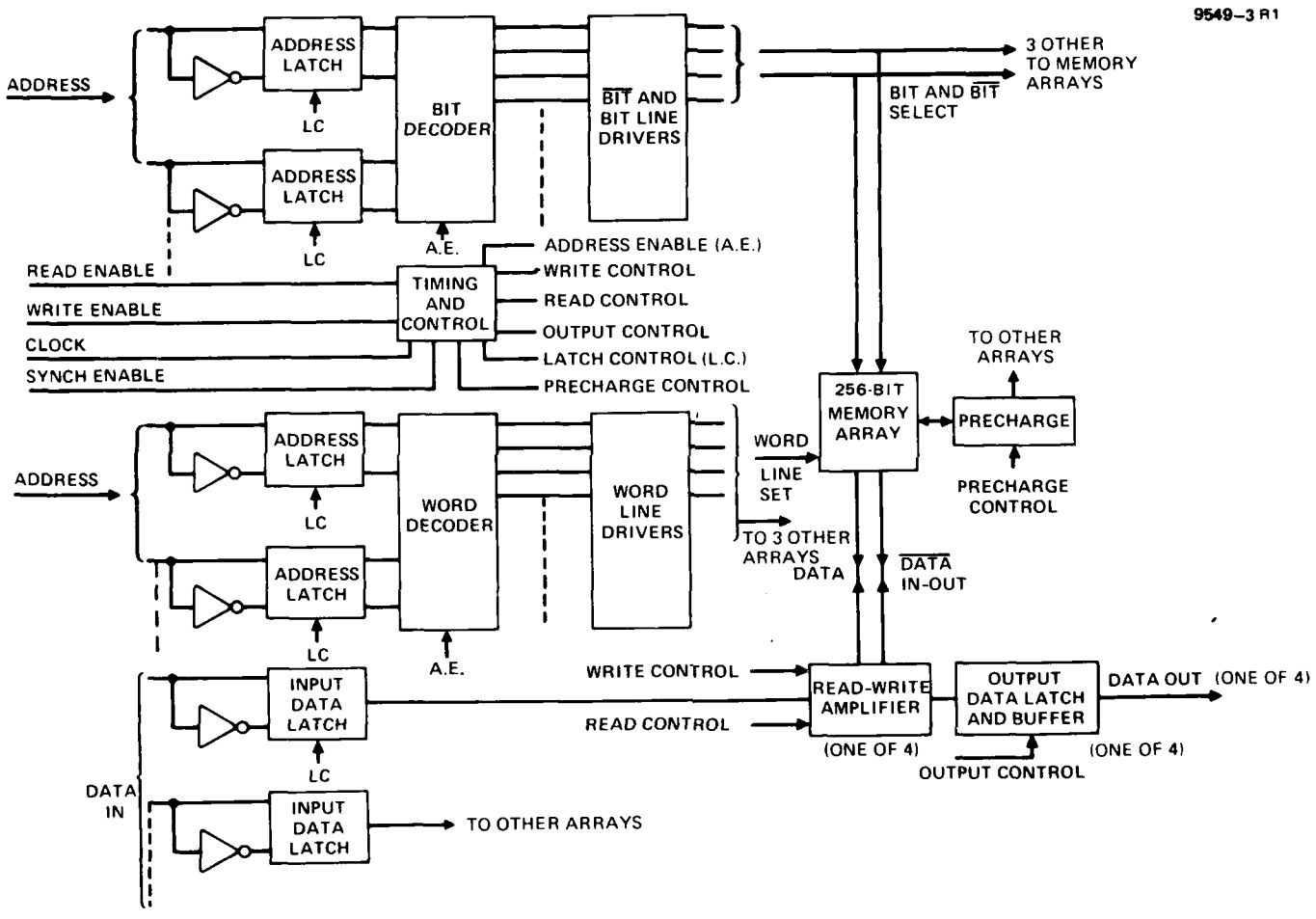


Figure 1-1. 1-K static RAM block diagram.

Besides the enhancement of operational flexibility by providing for either synchronous or asynchronous operation, the input latches have two other potential advantages:

- The enable signals can be used to define the time at which the input data and address are stable. This can minimize the probability that system glitches on these lines give false information.

- The provision of an output data latch eases somewhat the testability of the access times. An optional output latch signal could be provided to latch the output data after a given delay. This in effect puts the output strobe on chip and allows the output test circuitry to function at a slower rate.

The 1-K RAM consists of four 16 x 16 cell arrays driven (in the 256 x 4 arrangement) by 16-word-select driver circuits and 16 bit-select driver circuits. Each cell is a cross-coupled pair of inverters (or set-reset flip flop). Several implementations of the cell are given in the next section. The word- and bit-select drivers are driven by the address decoders. For a 16 x 16 array, each of these decoders is a 5-input gate with appropriate connections to four of the word-address or bit-address signals from the output of the address latches. The fifth input is an address-enable input. The address latches are driven in turn by the address inputs and the complementary address inputs generated by the input inverters.

In the read mode, the timing and control circuits provide a read-enable input to the sense amplifier circuitry and a disable signal to the precharge circuit, which then floats the bit lines. This sense circuitry perceives the differential current drawn from the bit and $\overline{\text{bit}}$ lines to the cell. (Single line sensing would be possible but would be less immune to voltage and device parameter variation.) To minimize the required voltage change on the high-capacitance bit lines, the sense amplifier must provide a high voltage gain. We have chosen a high-gain differential amplifier with bit and $\overline{\text{bit}}$ line inputs. The output of the differential voltage amplifier is then used to drive the output data latch.

The latch signals are derived from the timing and control circuit, with the timing dependent on synchronous or asynchronous operation. In synchronous operation, the output data are latched on the introduction of the enable

signal, coincident with new address input. In asynchronous, or normal, operation, the output data are latched after the access delay. On latching the output data, the precharge to the bit lines is turned on in preparation for the next cycle. The precharge overlaps the setup of the input latches and drivers.

In the write mode, the bit- and word-driver sequence is the same as in the read mode. However, the write-enable signal is used in the timing and control logic to generate signals that disable the read sense amplifier, turn off the precharge, and enable the write amplifier. The write amplifier, with inputs from the input data latch, resets the selected cell by driving the appropriate bit or $\overline{\text{bit}}$ line low and the other line high.

SECTION 2

MEMORY CELL

A. POSSIBLE CELL CONFIGURATIONS

Figure 2-1 shows four cross-coupled inverter circuits, or set-reset flip flops, that were considered for use as the basic memory cell. These cell implementations include several types of inverters:

- Depletion-mode Schottky-barrier FET logic (SDFL) inverters[1]
- Enhancement-mode (ENFET) inverters
- Quasi-normally-off inverters.[2]

The ENFET cells are of primary interest because they would dissipate the lowest power; however, they also have the most stringent processing requirements. Buffered depletion-mode FET (DFET) cells[3] were not included because of their high power dissipation. The SDFL and quasi-normally-off circuits are of potential interest because of their less stringent processing requirements and because their power dissipation generally falls mid-range between those of ENFET circuits and buffered DFET circuits.

The cell in Figure 2-1(a) is based on cross-coupled SDFL inverters. Word-line addressing is controlled by the voltage on the gates of the two word-address transistors. Bit-line addressing is controlled by the bit- and $\overline{\text{bit}}$-select transistors, which connect or disconnect a column from the sense amplifier. Bit-line addressing could also be implemented using a current-steered source-follower configuration similar to that shown in Figure 2-1(b). The component count in this cell is eight transistors and two diodes.

The cell in Figure 2-1(b) is based on the enhancement-mode inverter. Word addressing is accomplished by raising the drain and source potential of a row of cells. Column addressing is accomplished by turning on the bit-line select transistor, thereby connecting the line to a current source. The current drawn by the current source is supplied by either the cell address FET or the bit-line reference FET, depending on the memory state of the cell. The reference transistor comprises a current-steered source follower. The sense circuitry detects whether the bit or $\overline{\text{bit}}$ line is drawing current through its

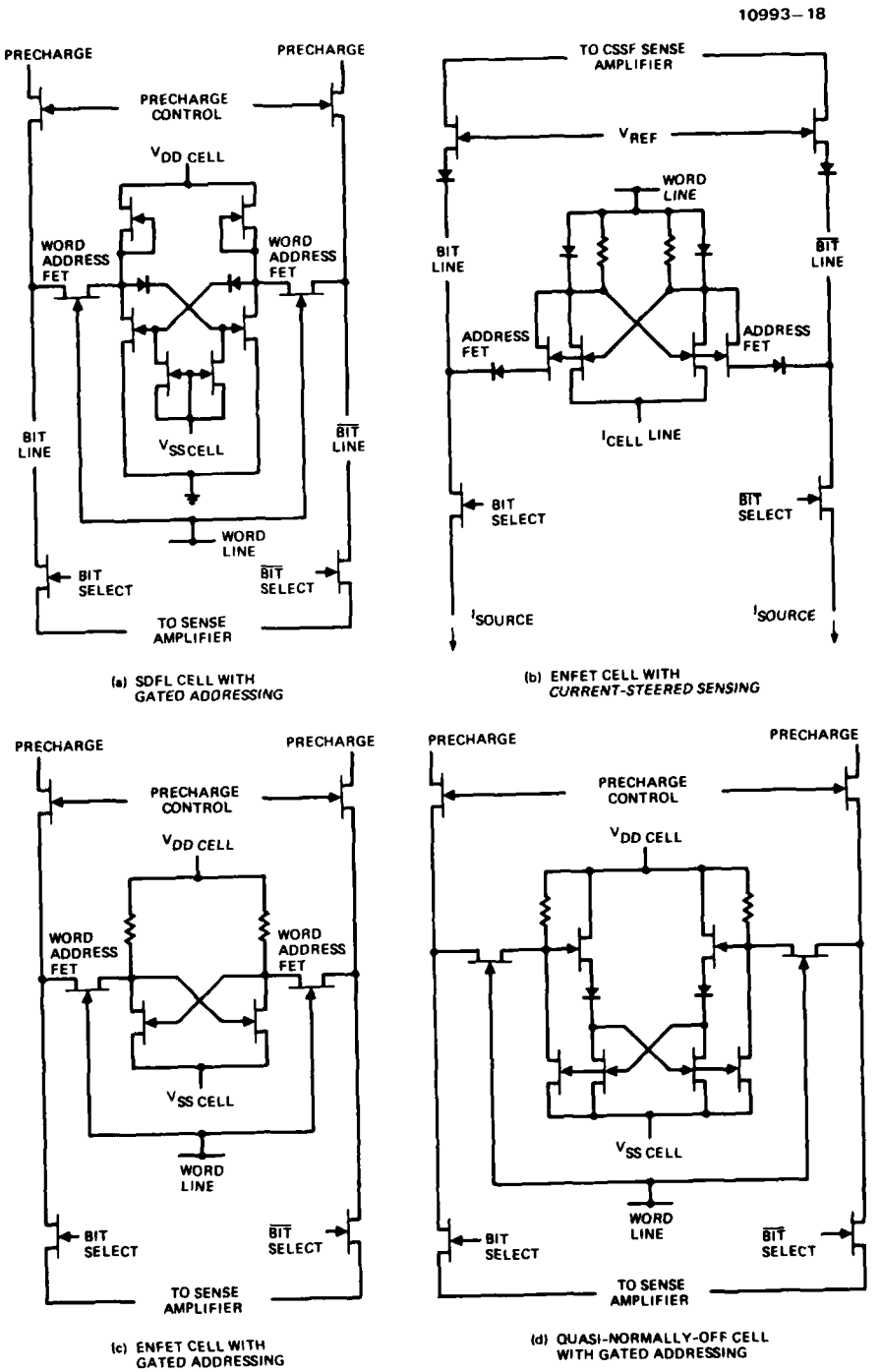


Figure 2-1. Static memory cell approaches.

reference transistor. The component count is four transistors, two resistors, and four diodes.

The cell in Figure 2-1(c) is an enhancement-mode cell that uses gated word-line addressing similar to that of Figure 2-1(a). In operation, both of the bit lines are precharged to a voltage equal to the internal cell node voltage of the offside inverter (∿0.5 V). Either the bit line or the $\overline{\text{bit}}$ line is then discharged through the on-side of the addressed cell. The state of the cell is sensed either by detecting the resulting voltage difference between the bit and $\overline{\text{bit}}$ lines or by sensing the current drawn from the bit line by the on-side transistor (by using a transconductance sense amplifier). The component count is four transistors and two resistors.

The cell in Figure 2-1(d) employs quasi-normally-off (QNO) MESFETs. This cell, like the ENFET cell, requires only a single supply voltage. It uses transistors operating as enhancement-mode devices but is designed to be less sensitive to pinch-off voltage variations than the ENFET cells of Figure 2-1(b) and (c). Typical QNO pinch-off voltages range from -0.4 V to 0.1 V. This cell requires eight transistors, two diodes, and two resistors. Alternative QNO configurations are available.[2]

In order to compare these several cell configurations, the following analyses were made.

1. ENFET Cell with Gated Word Addressing

Figure 2-2 shows a more detailed configuration of the ENFET inverter cell using gated word-line (or row) addressing. To minimize the read-response time, it is necessary to change the voltages on the bit lines as fast as possible. This requires:

- Maximizing the differential current from the bit and $\overline{\text{bit}}$ lines
- Minimizing the capacitances of the bit lines, the bit bus line, and the devices connected to these lines.

The bit line voltages can be altered in two ways by the state of the cell:

- The initial bit and $\overline{\text{bit}}$ voltages could be low, i.e., near the drain voltage of the on-side memory cell ENFET (∿0 V). In this case,

reference transistor. The component count is four transistors, two resistors, and four diodes.

The cell in Figure 2-1(c) is an enhancement-mode cell that uses gated word-line addressing similar to that of Figure 2-1(a). In operation, both of the bit lines are precharged to a voltage equal to the internal cell node voltage of the offside inverter (∿0.5 V). Either the bit line or the $\overline{\text{bit}}$ line is then discharged through the on-side of the addressed cell. The state of the cell is sensed either by detecting the resulting voltage difference between the bit and $\overline{\text{bit}}$ lines or by sensing the current drawn from the bit line by the on-side transistor (by using a transconductance sense amplifier). The component count is four transistors and two resistors.

The cell in Figure 2-1(d) employs quasi-normally-off (QNO) MESFETs. This cell, like the ENFET cell, requires only a single supply voltage. It uses transistors operating as enhancement-mode devices but is designed to be less sensitive to pinch-off voltage variations than the ENFET cells of Figure 2-1(b) and (c). Typical QNO pinch-off voltages range from -0.4 V to 0.1 V. This cell requires eight transistors, two diodes, and two resistors. Alternative QNO configurations are available.[2]

In order to compare these several cell configurations, the following analyses were made.

1. ENFET Cell with Gated Word Addressing

Figure 2-2 shows a more detailed configuration of the ENFET inverter cell using gated word-line (or row) addressing. To minimize the read-response time, it is necessary to change the voltages on the bit lines as fast as possible. This requires:

- Maximizing the differential current from the bit and $\overline{\text{bit}}$ lines
- Minimizing the capacitances of the bit lines, the bit bus line, and the devices connected to these lines.

The bit line voltages can be altered in two ways by the state of the cell:

- The initial bit and $\overline{\text{bit}}$ voltages could be low, i.e., near the drain voltage of the on-side memory cell ENFET (∿0 V). In this case,

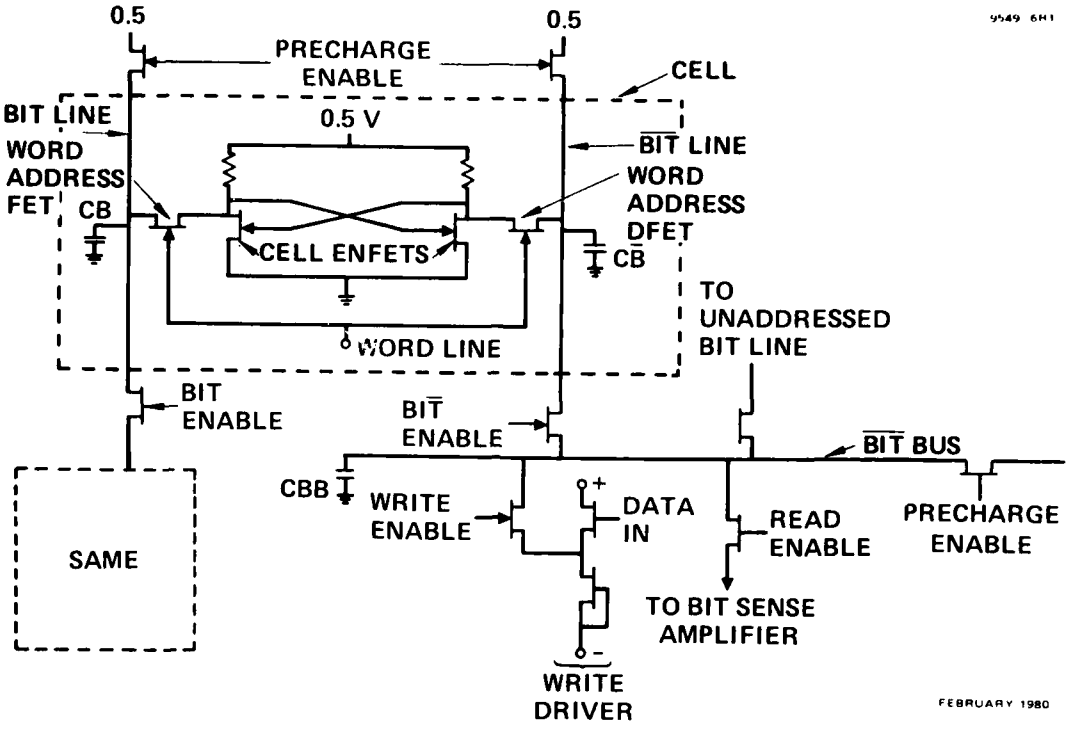


Figure 2-2. ENFET cell with gated addressing.

the off-side bit line of an addressed cell would be charged to the off-side drain voltage by drawing current through the load resistors.

- Alternately, the bit and $\overline{bit}$ lines could be precharged to the drain voltage of the off-side cell ENFET ($\sim$0.5 V). In this case, the on-side transistor of the cell would sink current from the corresponding bit line and drop its voltage toward zero.

The differential current from the bit and $\overline{bit}$ nodes can be greater in the latter case because the on-resistance of the cell ENFET is less than the resistance of the load resistor, particularly since one would like to keep the load-resistor value large to minimize the standby power dissipation of the cell. For this reason the precharge mode of operation was chosen for analysis.

In the design of the cell, consideration must be given to the possibility that the read current through the transistors in the addressed cell may cause the cell to assume an indeterminate state (i.e., a destruct-read may result).

This is controlled in our design by sizing the word address FETs to limit the read current through the cell ENFETs. Furthermore, the need to minimize the bit-line capacitance imposed by the drains of all of the address transistors associated with the nonaddressed rows of the array makes it desirable to achieve whatever maximum read-current is allowed with the smallest (and lowest capacitance) devices. For this reason, depletion-mode FETs (DFETs) are chosen for the word address FETs in the cells.

A dc simulation of the cell operating points was performed using a SPICE2 analysis. Various size address DFETs (with a pinch-off voltage V_p = -1 V) were used in a series of simulations to determine the maximum read current allowed through the cell and the size of the corresponding DFETs. The modeling parameters of the ENFETs (25-μm wide) were chosen to give transfer characteristics closely approximating the ENFET devices that have been fabricated in our laboratory.

The dc simulations led to the following results:

- The bit-line current can be ∿200 μA without a destructive read
- The width of the corresponding address DFET transistors is 10 μm.
- The bit-line current is not very sensitive to the size of the cell load resistor. A 50-kΩ load resistor was chosen.
- The standby power dissipation is 5 μW per cell with this load value.

These values were used in the subsequent transient analysis (Section 2.C).

2. Current-steered ENFET Cell

A corresponding dc analysis was performed for the ENFET cell (Figure 2-1(b)) using a current-steered source follower as the address transistor. In this case, all the transistors in the cell were chosen to be 25-μm-wide ENFETs, with model parameters corresponding to our experimental results. The reference FETs were also chosen to be 25-μm-wide ENFETs. The SPICE2-simulated-current differential is about 100 μA, if a maximum limit of 0.5 V is imposed on the forward bias of all transistors. This low value of read current is due to the limited current-sourcing capability of the address FET with a low drain voltage (∿0.1 V).

Because of its higher bit-line current capacity, the gated-address ENFET cell configuration has been selected as the superior implementation.

3. SDFL and Quasi-Normally-Off Cells

Based on simulations, an SDFL inverter with 5-μm-wide transistors would consume about 0.5 mW. Published results on quasi-normally-off inverters indicate a power dissipation of 0.15 mW for an inverter with 5-μm-wide devices.[2] To first order, these values would also be the approximate power dissipations of the memory cells.

B. CELL SELECTION

The factors that contribute to a choice between the approaches are:

- Cell size or array density
- Cell complexity
- Peripheral circuit complexity
- Speed performance
- Power performance
- Fabrication difficulty.

Table 2-1 gives a tabulation and rating for the various approaches.

The ENFET cell has the advantage of moderate cell complexity and excellent, low standby power requirements. As far as the array power dissipation is concerned, this technology is clearly extendable to large arrays; the two performance, or design issues, are the read-sense time and the potentially lower noise immunity due to reduced logic swing. The latter problem requires a careful design that minimizes feedthrough to the internal cell nodes. The read-time issue has been addressed in the simulations that are reported below, and the values found are acceptable for fast (1-nsec) RAMs.

Another issue is that the ENFET approach requires the development of a compatible ENFET-DFET-diode technology. However, this technology should probably be developed in any case because of the increased flexibility it will give the circuit designer in the development not only of RAMs but also of other

Table 2-1. Comparison of Memory Cell Approaches

Criteria \ Cell Type	SDFL	ENFET	Quasi Normally Off
Cell Complexity	High 8 Transistors 2 Diodes 3 Power Lines	Moderate 4 Transistors 2 Resistors 2 Power Lines	High (Several Options[2]) 8 Transistors 2 Diodes 2 Resistors 2 Power Lines
Cell Size	Moderate	Moderate	Probably High
Peripheral Circuit Complexity	Moderate	Moderate	Moderate
Speed	O.K. Probably fastest read time	O.K. (See Read & Write *simulation*)	O.K.
Power Dissipation	∿0.5 mW standby per cell (depends on design details). Power down may be possible. Marginal for ≥1K (0.5 mW assumes 5-μm FETs, logic swing 1.3 V)	∿5 μW per cell (25-μm-wide ENFETs)	∿0.15 mW/cell (5-μm-wide cell FETs) Power down may be possible
Fabrication Difficulty	Planar DFET wafer technology – Pinchoff uniformity may be a problem	Requires compatible DFET-ENFET technology. Close matching of ENFETs within a cell	FET matching may be less stringent. Requires compatible DFET-ENFET technology
Performance Reliability		Low internal logic swing reduces noise margin	
	Latched addressing increases system reliability		

LSI circuit functions. In particular, if circuit count exceeds $\sim 10^3$ gates, a low-power approach such as ENFET logic becomes desirable.

The disadvantages of the SDFL and QNO cells are the relatively high cell complexities and the higher power dissipations.

The low cell complexity and very low standby power of the ENFET cell have led us to select it as the preferred design. A possible physical layout of such a cell is shown in Figure 2-3. This cell is based on the use of 1 x 25-μm-gate ENFETs in the flip flop, 1 x 10-μm DFETs for the word address transistors, and 50-kΩ load resistors. These values come from a simulation of the ENFET static cell. The total cell, including bus leads, is 42 x 48 μm^2 (area = 3.1 mil^2). The design rules used in the cell layout were:

- Linewidth = 2 to 4 μm
- Line-to-line separation = 2 μm
- Source-drain length = 4 μm
- Gate length = 1 μm
- Source-drain separation = 5 μm

C. TRANSIENT ANALYSIS

This section presents the results of detailed transient simulations of the designs which have been developed for the static RAM cell and for the read and write circuits. Other required peripheral circuits, such as the input/output data latches, address decoders-line drivers, and precharge drivers,are discussed in Section 3.

1. Read Mode

a. Cell Response

The key parameter required for the transient analysis is the total capacitance loading the bit lines and the bit-bus lines. This capacitance is made up of several components:

- The bit-line capacitance to ground and to adjacent lines

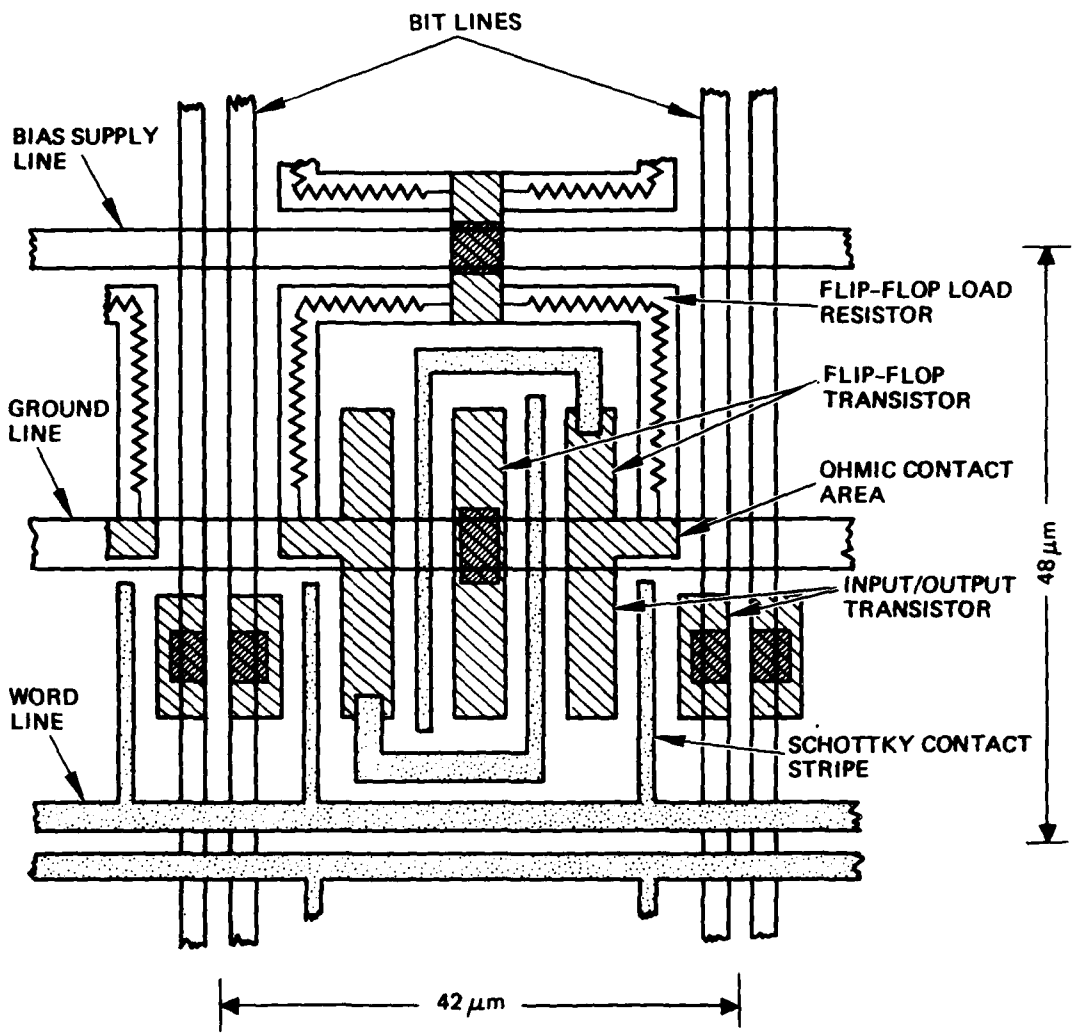


Figure 2-3. Layout of ENFET static RAM cell.

- The total drain capacitance of the address transistors of the 15 nonaddressed cells connected to the bit line (assuming a 16 x 16 array)
- The total drain capacitance of the 15 nonaddressed bit-enable transistors
- The gate capacitance of the bit-enable transistor on the addressed line
- The source capacitance of the precharge transistor
- The drain capacitance of the write-enable transistor
- The gate capacitance of the read-enable transistor
- The gate capacitance of the sense-amplifier input transistor
- The source capacitance of the precharge-enable FET.

Estimation of the line capacitances requires some assumptions. If we assume a 50-μm-square cell, a 16 x 16 memory array would require that both the bit line and the bit-bus line each be at least 800 μm long. For the simulation, we assume a total line length of 2000 μm, a linewidth of 1 μm, and a line spacing of 2 μm. For this case, the line capacitance to ground would be ∿0.11 pF per 1 mm of line length, or 0.22 pF total for the line. This line capacitance is shown in Table 2-2 along with the estimated values for all of the contributing device capacitances listed above. The total capacitance loading of the bit and $\overline{\text{bit}}$ nodes are assumed to be 0.4 pF in the simulations.

Table 2-2. Read-Mode Capacitance Loads

Line Capacitance	0.22 pF
Cell address FETs (15 x 0.00176 pF)	0.026
Bit-bus address FETs (15 x 0.0044 pF)	0.066
Addressed bit FET	0.032
Precharge FET	0.0044
Write-enable FET	0.0044
Read-enable FET	0.01
Sense-amplifier FET	0.01
Precharge-enable FET	0.0042
Total	0.38 pF

Using this capacitance load, a SPICE2 simulation of the bit and $\overline{bit}$ line responses was run using the following initial conditions:

- One cell ENFET on
- The other cell ENFET off
- The bit and $\overline{bit}$ lines initially at 0.5 V
- The word-address line at 0 V.

The transient response of the bit and $\overline{bit}$ nodes following turn-on of the word address FETs is shown in Figure 2-4. Following an initial transient, the on-side voltage decreases as a near ramp-like function, with a decay rate of 0.5 V/nsec. This ramp was used in the following sense-amplifier simulation to give an overall read response simulation.

9549-7

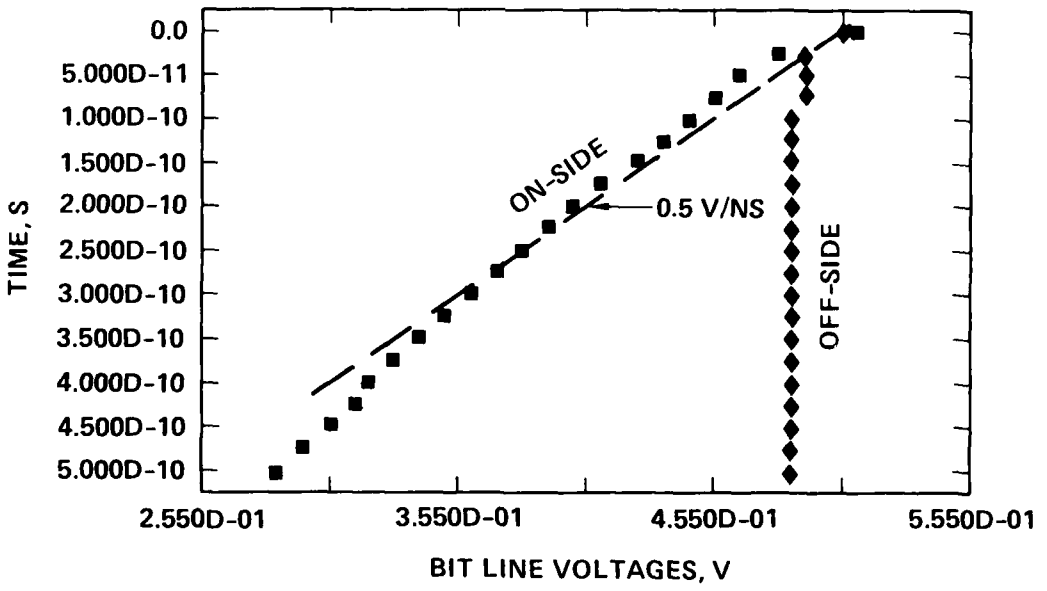


Figure 2-4. Bit and $\overline{bit}$ line transient response simulation.

b. Sense Amplifier and Total Read Response

As shown by the above simulation, the voltage slew rate on the bit and $\overline{\text{bit}}$ nodes is slow enough that, to achieve acceptable read times, the state of these two lines must be sensed well before the full voltage differential is reached.

Figure 2-5 is a differential amplifier with a gain of ∿20 (determined by the $g_m \cdot R_o$ product of the FETs). This circuit has been simulated in some detail. A dc transfer analysis (output voltage versus bit-line input voltages) was performed to set the size of the FETs and the operating voltages. All the FETs have -1 V pinch-off. The selected transistor sizes and operating voltages are as shown. The dc transfer characteristics for these conditions are shown in Figure 2-6.

The circuit design of Figure 2-5 does not, however, constitute a practical circuit because very small differences in the parameter values of the transistors will move the operating voltages into a region of low gain. Some method of stabilizing the dc operating point in the high-gain region is required. Moreover, the output voltages are unusual values that need to be shifted to provide standard logic levels (e.g., 0, -1) that can drive an output latch. Figure 2-7 shows the circuit as finally derived. The operating point is stabilized by providing a fixed reference bias to the load FETs of the differential amplifier through large resistors, R_{bias}. An effective ac short is maintained between the gates and sources by the bias capacitors. Fairly large values, ∿0.2 pF, are required to prevent an output droop for at least 2 nsec. The output source-follower stage provides a level shift to the latch driver levels (0, -1). The supply voltages V_{SS}, V_{SS2}, and V_{DD} are the same as those required by the other peripheral circuits.

Using these final design values, a SPICE2 simulation was run to determine the output response of the sense amplifier to a ramp decrease in voltage (from 0.5 V to 0.25 V in 500 psec) on one of the bit lines. This input condition corresponds to the bit-line response found earlier (Figure 2-4). The capacitive load on the output-sense nodes was 0.015 pF, which approximates the source-gate capacitance of a 10-μm FET at the input to the output data latch. The response is shown in Figure 2-8. The time to achieve the required output levels (0, -1) was 280 psec.

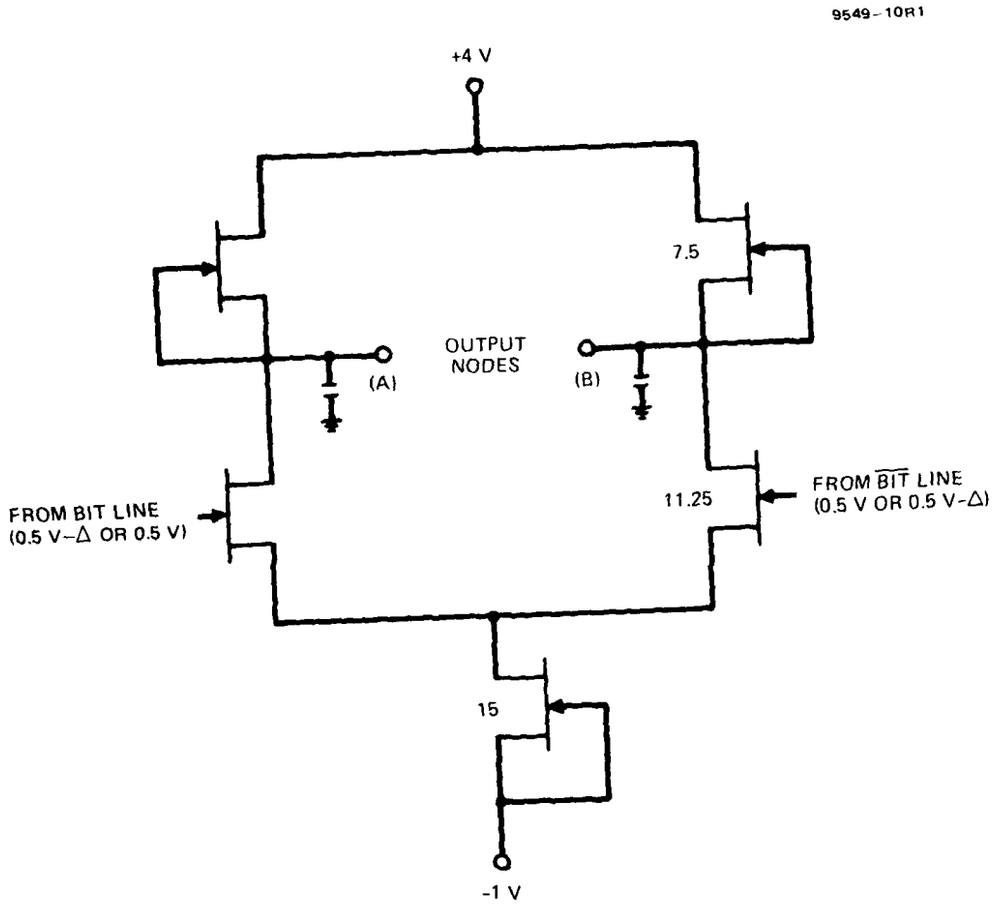


Figure 2-5. Differential sense amplifier. All FETs are 1-μm-gate DFETs (V_p =-1 V) and have the widths shown (in microns).

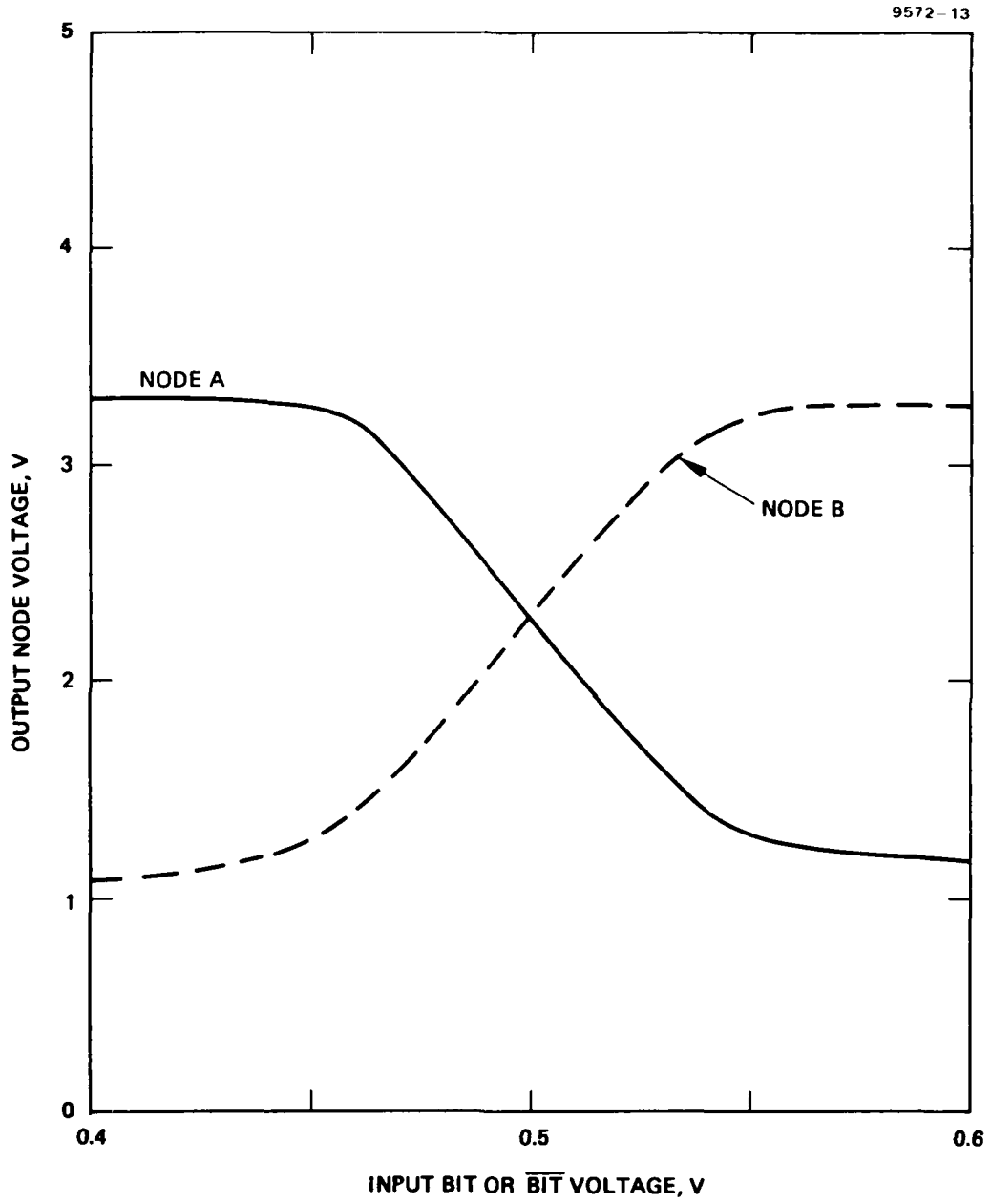


Figure 2-6. DC transfer characteristics of differential sense amplifier: One input at 0.5 V, second input is as shown.

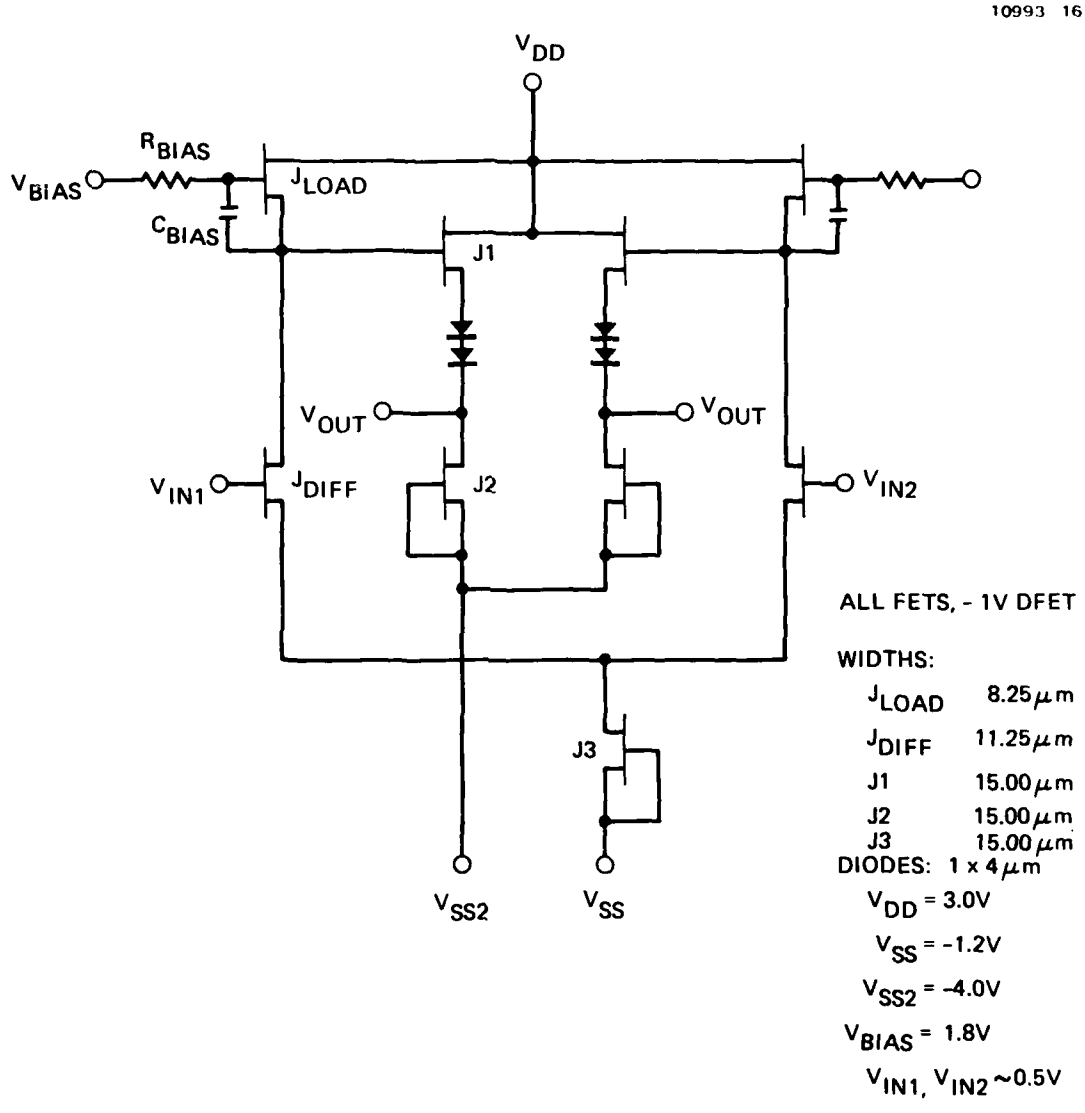


Figure 2-7. Final design of the differential sense amplifier.

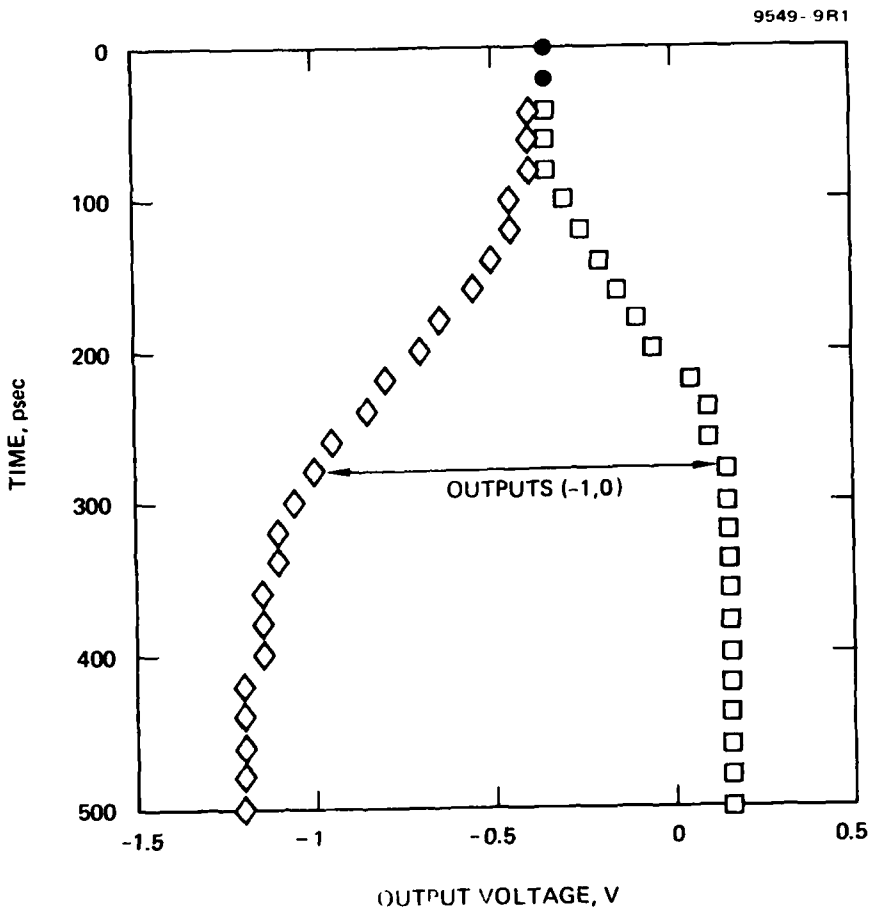
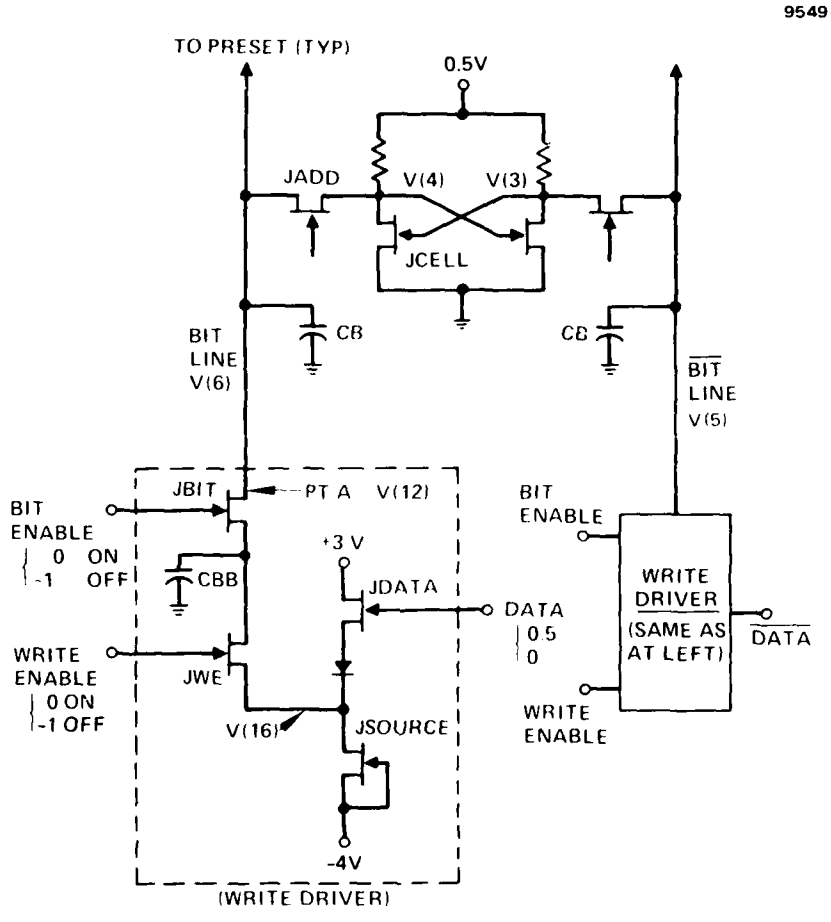


Figure 2-8. Simulated overall response of sense circuit.

2. Write Mode

Figure 2-9 shows the circuit that was simulated to determine the transient write-mode reset response. The capacitors CB and CBB (0.2 pF each) represent the loading by the unaddressed cells and bit lines.

A dc analysis was run to determine the appropriate FET widths for the operating biases. The bias values (+3, -4, -1.2, and +0.5 V) were chosen after iterating choices between the various circuits.



JCELL	25 μm EFET (VTO = +0.1V)
JADD	10 μm DFET (VTO = -1V)
JBIT	25 μm
JWE	50 μm
JDATA	50 μm
JSOURCE	50 μm

Figure 2-9. Simulated write circuit.

Table 2-3 shows the dependence of the internal cell voltages V(3) and V(4) on the bit-line voltage V(6) as it is decreased from 0.5 V to 0.4 V; bit is held constant at 0.5 V. The initial cell state has V(4) = 0.5 V and V(3) = 0.1 V. Under these conditions, the cell switches states very early (i.e., as the bit-line voltage drops to 0.46 V). Thus, to change the cell state, it is adequate to drive one bit line towards 0.5 V, by setting its data input at ∿0.5 V, and the other bit line towards 0 V, by setting its data input at ∿0 V. A write-enable gate voltage of 0 V was selected to minimize forward gate bias.

Table 2-3. Response of Memory-Cell Node Voltages to Decrease in Bit-Line Voltage: $\overline{Bit}$ = 0.5 V.

9572-15

BIT LINE	INTERNAL CELL NODES	
V (6)	V (4)	V (3)
5.000D-01	4.977D-01	1.940D-01
4.900D-01	4.889D-01	2.011D-01
4.800D-01	4.778D-01	2.105D-01
4.700D-01	4.645D-01	2.261D-01
4.600D-01	1.796D-01	4.977D-01
4.500D-01	1.760D-01	4.977D-01
4.400D-01	1.723D-01	4.976D-01
4.300D-01	1.687D-01	4.976D-01
4.200D-01	1.650D-01	4.976D-01
4.100D-01	1.613D-01	4.976D-01
4.000D-01	1.576D-01	4.976D-01

During the write mode, the write driver and memory cell are coupled by the currents flowing between the cell and the bit lines. Therefore, the entire circuit of Figure 2-9 was simulated for the analysis of the write transient response. A simulation was run to test both the set-up time and whether the cell, after being switched, would hold its new state. The assumed initial conditions were:

- Bit-enable gate = 0 V (on)
- DATA input = 0 V
- $\overline{\text{DATA}}$ input = 0.5 V

The write drivers have charged the bit and $\overline{\text{bit}}$ lines to 0.34 V and 0.5 V lines, respectively.

Starting with these initial conditions, the write-enable and data inputs are cycled as shown in Figure 2-10. To start the cycle (t = 0), the write-enable FETs are turned off, leaving the bit lines to discharge through the cell. At t = 500 psec, the data inputs are switched to their new values. At t = 1000 psec, the write-enable gate is turned on, and at t = 1400 psec, it is turned off again. This operation is designed to test whether the cell will hold its new state.

9549-12R1

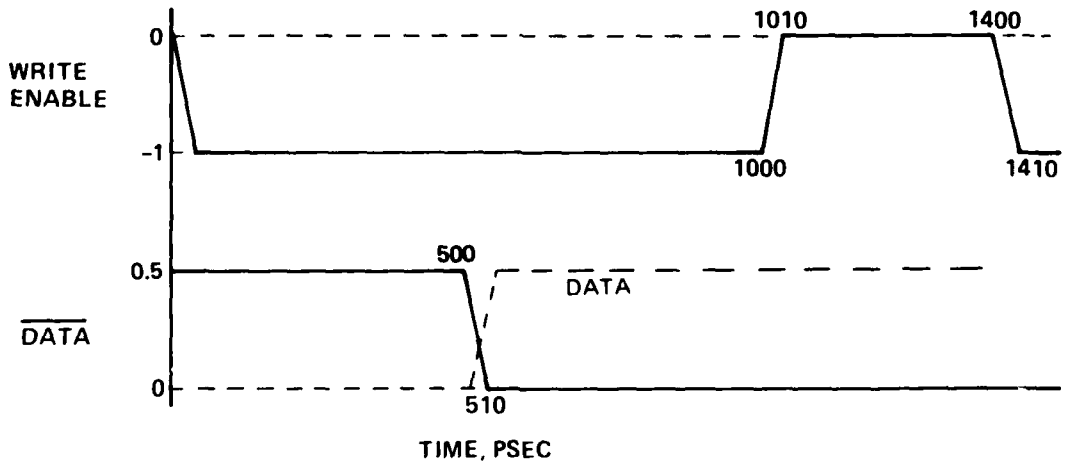


Figure 2-10. Control sequence for write simulation.

Figure 2-11 shows the results. Here, the crossover of the cell to a new state occurs at ∿350 psec after write enable, and the new state holds, if the write-enable signal is turned off after 400 psec.

In practice, the operations shown would overlap in time. One purpose of the analysis was to determine whether the initial write-enable and data-input transitions would influence the cell state; however, no adverse effects were noted. The drop in the voltage of the on-side cell transistor is an expected consequence of the discharge of the bit line through the memory cell transistor. The relatively low final voltage of the off-side (V4) results from the word-address switches being closed and no precharge being applied to the bit lines. The cell voltages will assume their normal levels following opening of the switches (unaddressing the cell) or precharging of the bit lines.

In conclusion, the simulations predict that an addressed cell can be switched to a new stable state within 400 psec of the application of the write-enable signal.

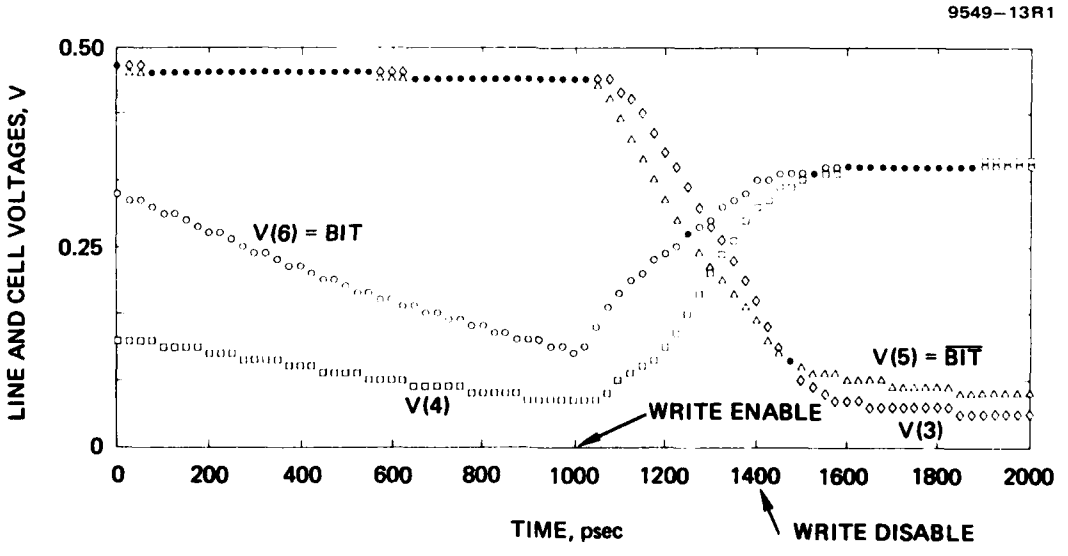


Figure 2-11. Simulated write-mode response.

D. ENFET PINCHOFF UNIFORMITY REQUIREMENTS

One of the key issues in the implementation of the ENFET static cell is the uniformity of the ENFET pinch-off voltages that may be required. A substantial difference in the pinch-off voltage of adjacent devices in a cell can cause the cell to lock up in one state. Further, if both devices have pinch-off voltages that are too high or too low, the cell can lose its bistable characteristic. In the dc analyses of the read and write modes, it is found that the most critical stability conditions occur during the read mode when the output nodes are connected to the precharged bit lines. We therefore analyzed the cell operating points during the read mode over a range of different pinch-off voltages (VT01 and VT02) for the two ENFETs in the cell. From this analysis, an acceptance window for VT01 versus VT02 was determined. Within this window, the cell state will be stable during the read operation (i.e., nondestructive readout). Figure 2-12 shows the allowable range of VT01 as a function or VT02. A fairly wide range of pinch-off voltages is allowed (-0.05 to 0.29 V) provided that the necessary match is maintained between the devices. The required quality of the match depends on the value of VTO, ranging from ±0.05 V at the center of the allowed eye to 0 V at the extremes. That is, over the array, a VTO variation of ±0.17 V is allowed, provided that the adjacent FET match is ±0.03 V over most of this range.

These tolerances are close to being met by our current ENFET fabrication process. Table 2-4 shows the results of ENFET pinch-off voltage V_p measurements made for several test-chip wafers fabricated at Hughes by ion implantation. Two of the wafers were fabricated by implanting directly into Cr-doped semi-insulating GaAs substrates grown by the horizontal Bridgeman (HB) technique. The third wafer was fabricated by implanting into a high-resistance buffer layer grown on an HB substrate by liquid-phase epitaxy (LPE). The global variations of V_p for the two HB wafers have standard deviations of about 90 mV. These variations have two major sources: (1) there are initial nonuniformities following implant and anneal, which are due to background impurities and thermal redistribution of the compensating Cr atoms; (2) the deep channel etch, which is used to produce a recessed-gate structure, accentuates the relative magnitudes of the initial variations and introduces

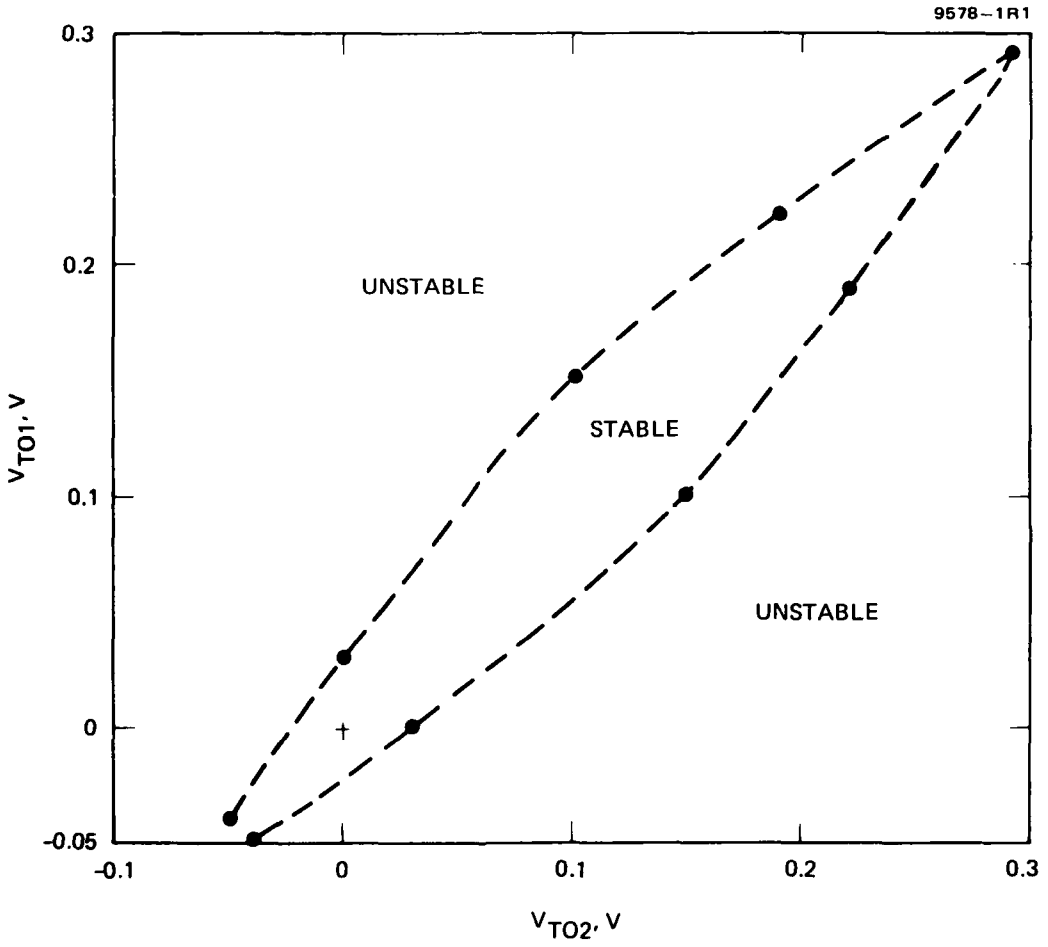


Figure 2-12. Stability conditions for ENFET cell during the read mode.

Table 2-4. Statistics of Pinch-off Voltage V_p Distributions

Substrate*	Global Distribution of V_p, mV		Difference in V_p Between Near Neighbors, mV	
	Median	Standard Deviation	Median	Standard Deviation
HB1	44	86	18	30
HB2	112	97	--	--
Buffer	44	415	42	239

*HB = Cr-doped horizontal Bridgeman

Buffer = Buffer layer grown on HB substrate by liquid-phase epitaxy

additional variations due to nonuniform etching. These global variations are significant for logic circuits of LSI complexity; however, the uniformity requirements relevant to memory-cell stability pertain to a pair of ENFET devices located in close proximity. Therefore, we also measured the pinch-off differences between neighboring 25-μm-wide ENFETs that are spaced 35-μm apart, center-to-center (Figure 2-13). The median difference in pinch-off voltage V_p between these neighboring devices is 18 mV, and the standard deviation of V_p is 30 mV. These variations are significantly less than the measured global variations and are close to the ±30 mV uniformity requirement predicted by the stability analysis of the memory cell. However, it must be remembered that the specified memory-cell uniformity represents an absolute limit rather than a standard deviation, so some improvement in processing uniformity, over that achieved to date with the HB material, will probably be required. Some of this improvement can be expected from the smaller spacing between memory-cell ENFETs, as seen in Figure 2-3 (i.e., ~12 μm spacing, center-to-center). The devices fabricated on the LPE buffer layer had considerably poorer uniformity than the HB devices, both globally and for near neighbors. This is mainly attributed to the fact that the LPE buffer layer had a poorer surface morphology (i.e., pits, hillocks, etc.) than the HB wafers. Additional buffer layer substrates should be evaluated, in

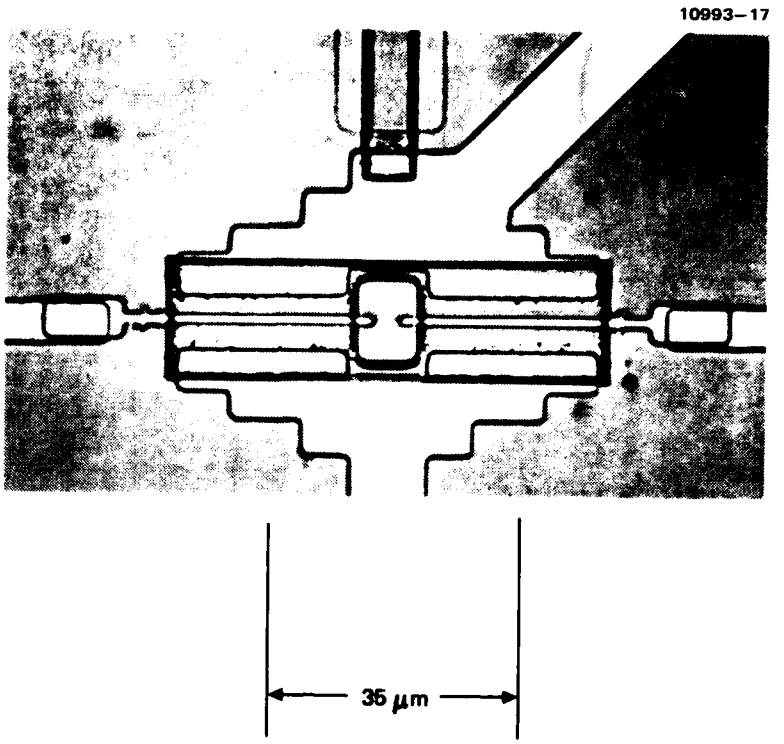


Figure 2-13. NOR-gate pair of 25-μm-wide ENFETs.

particular, layers grown by VPE. Undoped semi-insulating substrates grown by the liquid-encapsulated Czochralski (LEC) technique should also be evaluated.

SECTION 3

PERIPHERAL CIRCUITS

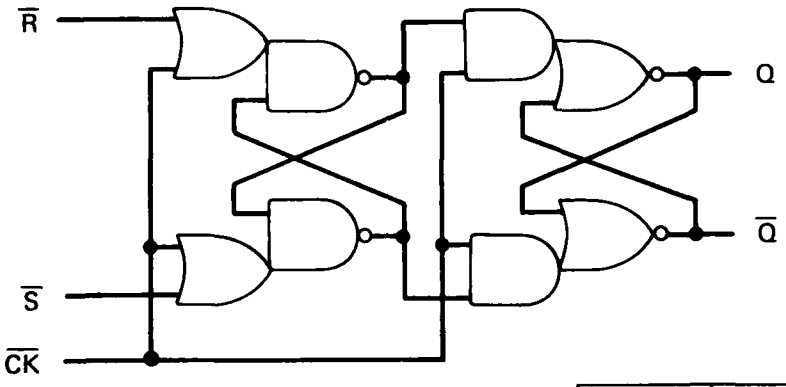
A. INPUT/OUTPUT LATCHES

A number of latch circuit configurations are available for the address- and data-input latches and for the data-output latches. At the speed required of the memory, it is desirable to implement these functions on-chip rather than with off-chip buffer latches. On the test chip (Section 5), the latches are implemented as master-slave flip flops (Figure 3-1) for increased flexibility in testing. In the actual RAM circuit, only one of the latch stages of the master-slave flip flops would be used. The flip flop incorporates a master latch based on the merged OR-NAND logic gate of Figure 3-2(a), and a slave latch based on the merged AND-OR gate of Figure 3-2(b). Due to the merged logic construction, either of these latches has one gate delay (plus an inverter delay necessary to generate a complementary input).

B. ADDRESS DECODERS AND LINE DRIVERS

The proposed address decoder is shown in Figure 3-3. It is essentially a 5-input SDFL NOR gate, selected because of its high fan-in capabilities. Four of the inputs are derived from the address latches; the fifth input is derived from the address-enable signal and prevents addressing of the array unless the enable signal is present. The circuit differs only from the usual SDFL NOR gate in that the output level must match the required driver levels rather than another gate. In the selected cell configuration (Figure 2-2), the required output voltages for the line drivers are 0 V for an addressed line (i.e., all inputs to its decoder are low) and -1 V for a nonaddressed line. The same circuit is used for both the bit- and word-select decoder-drivers, except the widths of the buffer- and driver-stage FETs are changed to account for the particular output load on the driver. Each word-address driver load includes 128 10-μm-wide DFETs on each word-address line (counting four 16 x 16 arrays), whereas each bit-select driver load includes eight select transistors on the bit and $\overline{\text{bit}}$ lines of the four 16 x 16 arrays.

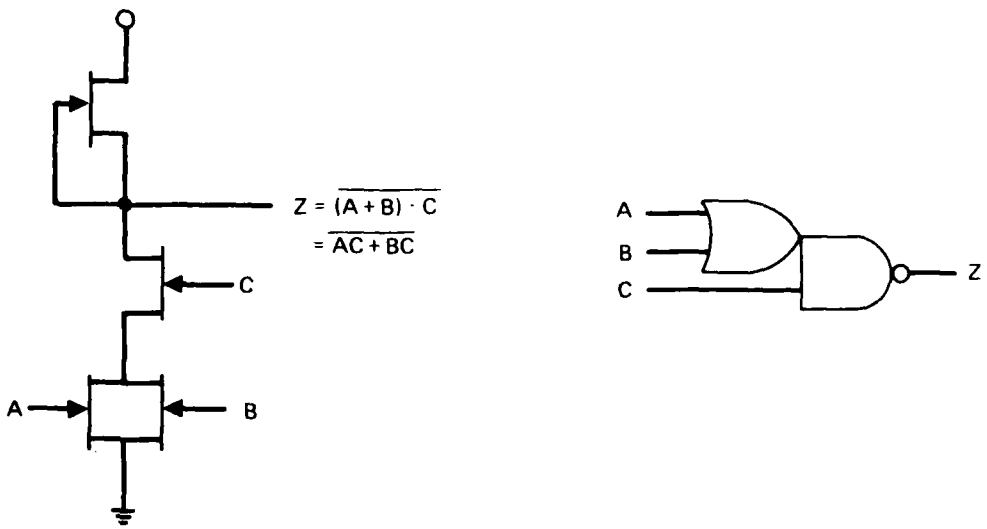
10719-2



$\overline{S}_n$	$\overline{R}_n$	Q_{n+1}
0	0	?
0	1	1
1	0	0
1	1	Q_n

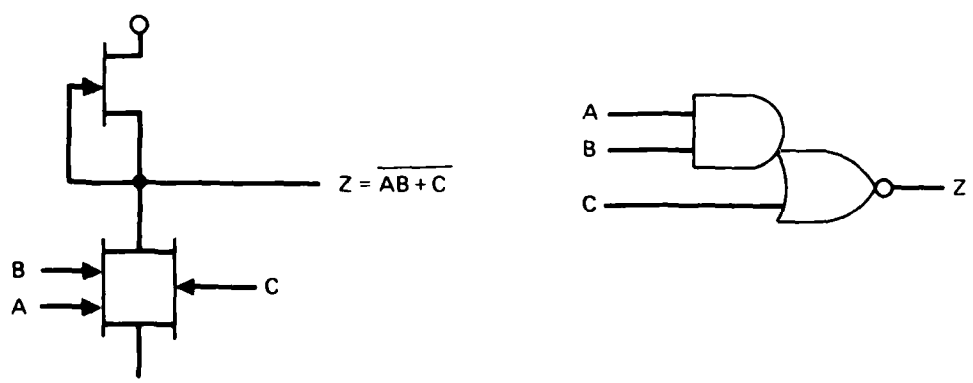
Figure 3-1. Master-slave flip flop.

10929-8



a. MERGED OR–NAND GATE

10929-12



b. MERGED AND-NOR GATE.

Figure 3-2. Merged two-level logic gates used in flip flop.

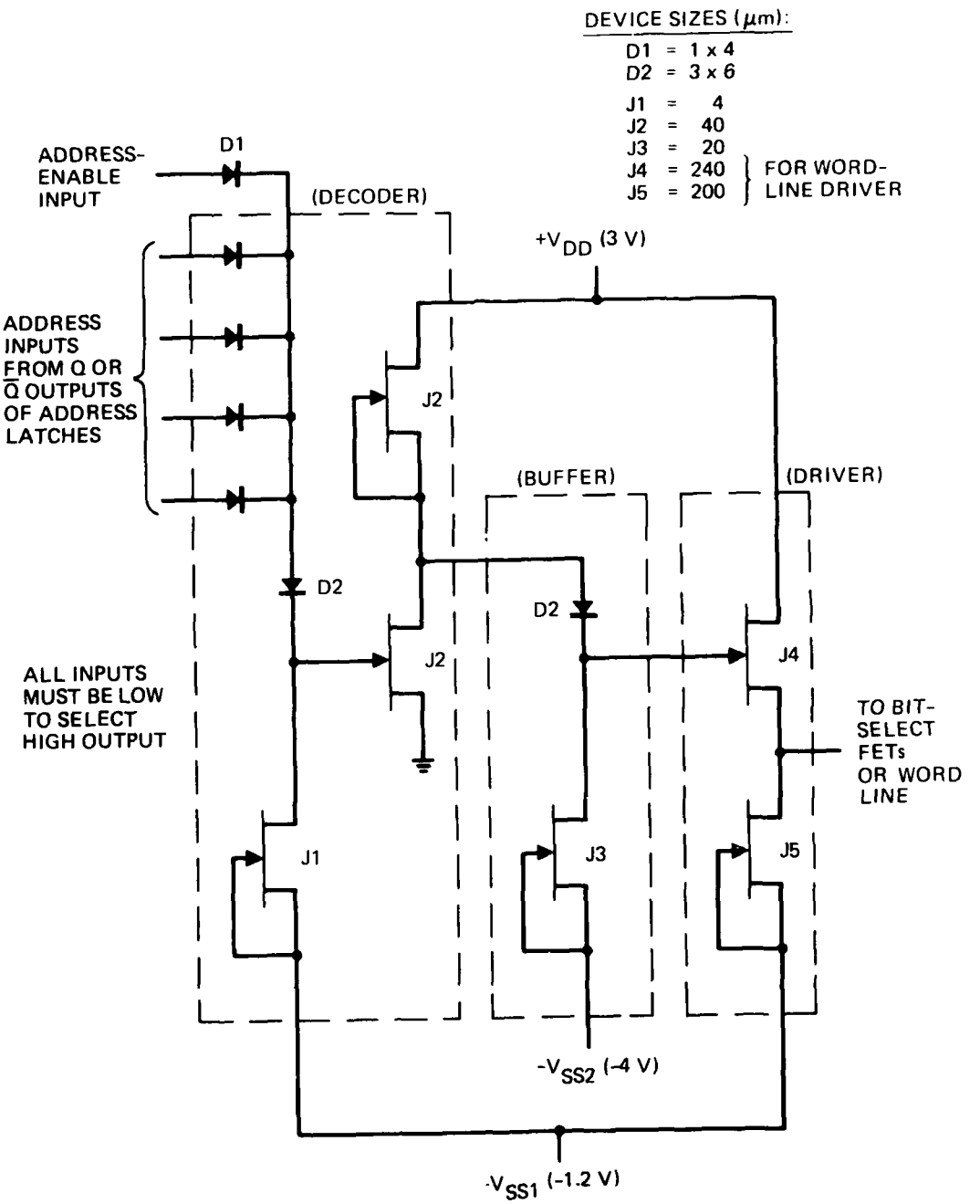


Figure 3-3. Address decoder and line driver — one of thirty-two decoder-drivers needed for a 16 x 16 array.

The design of the driver chain is important to power dissipation. The capacitive load imposed by the driven circuit, particularly the word-line address FETs, necessitates a large current drive to switch the voltage on the selected line within a subnanosecond time frame. If driven by the usual source-follower stage, the standby power for the driver would be excessive (at least several watts). In order to minimize the driver standby power, the buffer and driver stage circuitry, shown in Figure 3-3, was developed. Two different source-voltage supplies are used, such that the output-source driver gate is heavily biased off during standby and thus draws negligible current. This condition is achieved by using a more negative source supply on the buffer stage than on the output source-follower stage. The supply voltages selected (+3 V, -1.2 V, and -4 V) are identical to those used for the other circuits in the memory.

The circuit shown in Figure 5-9 was simulated to determine the transient response of the word-line decoder-driver chain. This circuit is the one implemented on the test chip and includes simulations of the output stages of the address latches (each four-times normal width to simulate all four address inputs) and a large diode logic stage (15-times normal) to simulate the 15 alternate channels in the address decoder. Only one buffer and output driver stage is implemented. By appropriate weighting of the computed currents for the three source-voltage and drain-voltage supplies, the total standby power for the word-line decoders and drivers (all 16 lines) is computed to be 290 mW. Note that this includes the power consumed by the output stages of the address latches. The computed transient response to an address-enable input is shown in Figure 3-4. The total delay between the state change in the address-enable input and the word line reaching its required state (0 or -1 V) is 520 psec. Essentially identical transient response results were obtained for a bit-line decoder-driver with scaled-down buffer and driver FETs. The total standby power for the 16 bit-line decoder-drivers is computed to be 87 mW.

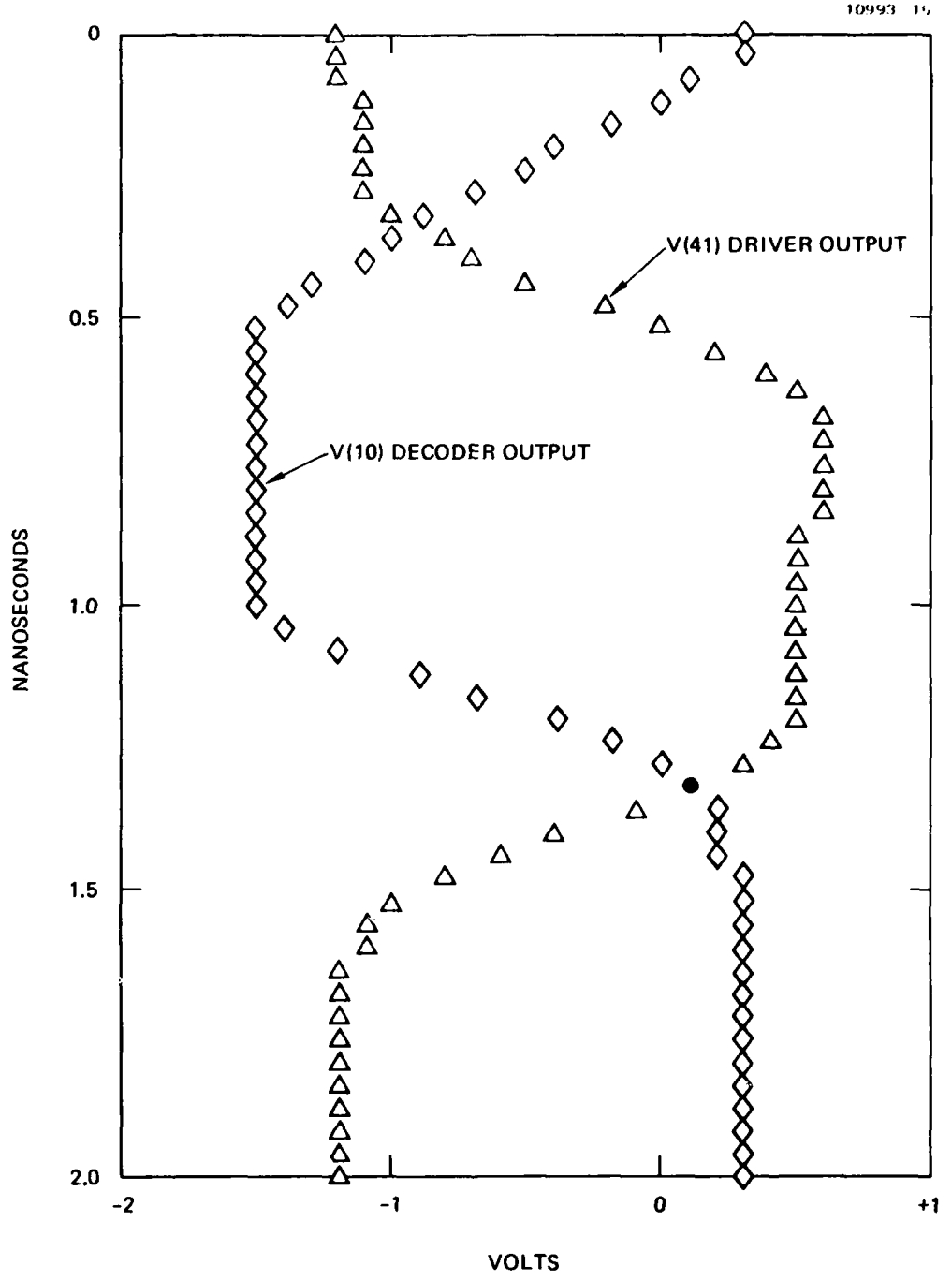
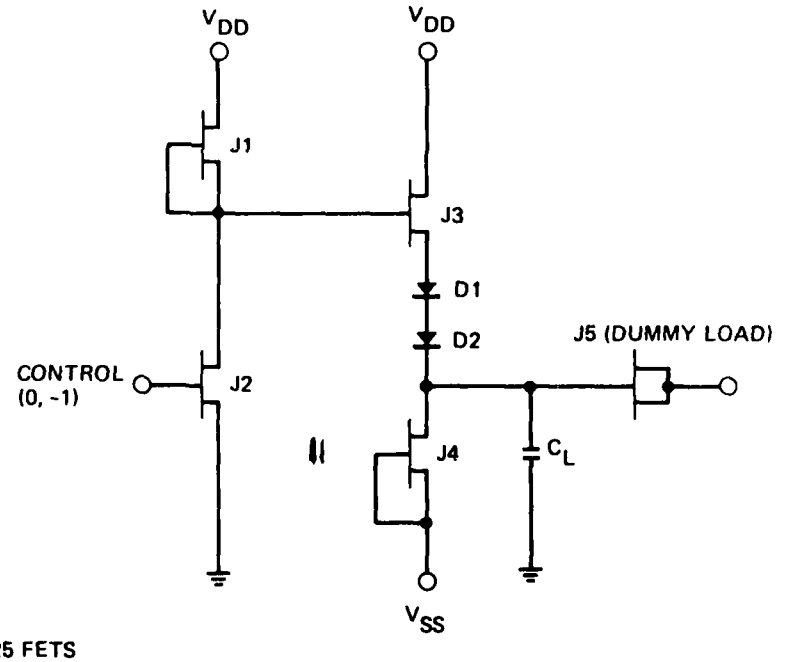


Figure 3-4. Transient response of word-line decoder and driver.

C. BIT-LINE PRECHARGE DRIVERS

The precharge-enable signal which controls the gates of the bit-line precharge FETs (Figures 2-2 and 2-9) switches from +0.50 V to -1.0 V when the array is addressed for read or write (i.e., the precharge is disconnected). This swing is in the opposite direction to that required on the bit and word address lines. The easiest way to implement the precharge-enable driver and to incorporate the required level shifting is to use a standard DFET inverter as the reset gate driver. Figure 3-5 shows the precharge gate driver, as simulated. The circuit dissipates 100 mW. The transient response is shown in Figure 3-6. The precharge gate turns off (-1 V) about 520 psec after the control signal goes high. The initiation of precharge-off and the setup of the address lines can be overlapping functions.

10993-14



-1V DFETS:

J1	1 x 10
J2	1 x 30
J3	1 x 240
J4	1 x 240
J5	1 x 3200 (128 1 x 25 FETS IN 4 16 x 16 ARRAYS)
D1	4 x 40
D2	4 x 40

C_L = 0.4 pF

V_{DD} = 3

V_{SS} = -4

Figure 3-5. Precharge gate driver.

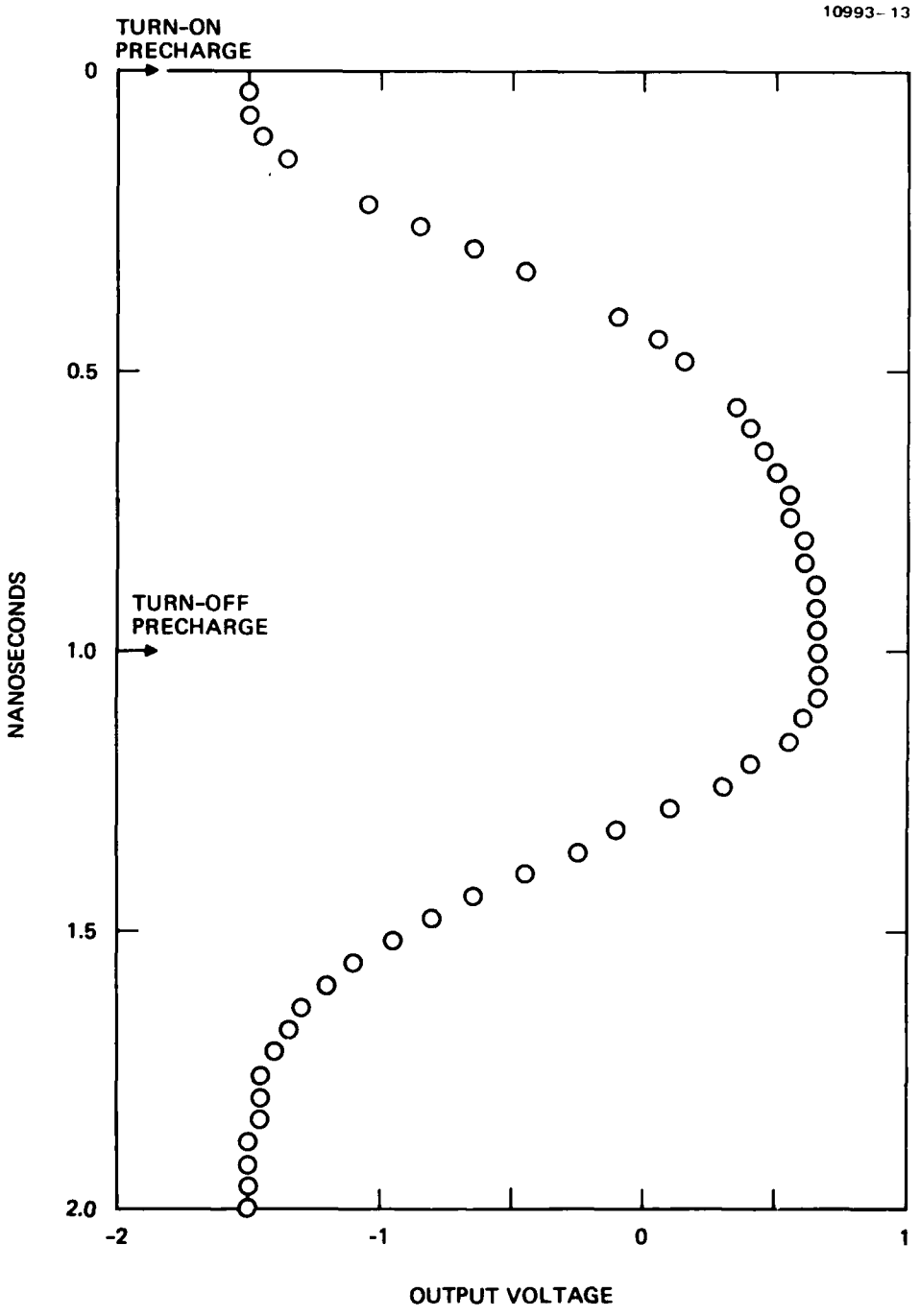


Figure 3-6. Simulated transient response of the precharge driver: control on at t = 0; off at t = 1 nsec.

SECTION 4

TIMING AND POWER BUDGETS

A. TIMING BUDGET

The times required for the key operations are summarized in Table 4-1. The I/O latch operations have not been analyzed in detail and so are stated in terms of equivalent gate delays; in DFET logic, a typical gate delay is about 70 psec. For a straight-forward addition of the individual delays, the calculated total access times slightly exceed 1 nsec; however, some overlap of the functions will be allowed. Moreover, we have included the I/O data- and address-latch functions on the chip as part of the RAM access sequence. Some further time savings can probably be achieved in these areas by more efficient operational sequencing and circuit design. Thus, based on our simulation analyses of the initial memory circuit designs, the 1-nsec access time for a 1-kbit GaAs RAM appears realizable.

Table 4-1. Timing Budget

Operation	Read Mode	Write Mode
Generation of complementary inputs (ADDRESS and $\overline{\text{DATA}}$)	1 gate delay	1 gate delay
Latching of address and data inputs	1-2 gate delays	1-2 gate delays
Address decoding and set-up of bit and word lines (includes delay of latch output stage)	520 psec	520 psec
Precharge turn-off (simultaneous with address selection)	520 psec	520 psec
Read sense response	320 psec	N/A
Write reset response	N/A	370 psec
Latching of output data	1-2 gate delays	N/A
Total time	$\leq$840 psec plus 3-5 gate delays	$\leq$890 psec plus 2-3 gate delays

B. POWER BUDGET

Table 4-2 summarizes the power estimates that were provided by the SPICE2 simulations for a 1-k RAM consisting of four 16 x 16 memory arrays. The I/O latches and timing and control circuitry were not simulated, but the table includes estimates of their power requirements. The I/O power is estimated on the basis of eight address latches and eight data latches dissipating approximately 15 mW per latch. The timing and control estimate is based on an assumption of 10 equivalent gates and about 10 mW per gate. As noted earlier, the major problem in developing a design with a power budget under 1 W was the required reduction in standby power for the word- and bit-address drivers. This problem was solved with a buffer-driver stage using two different source supply voltages.

Table 4-2. Power Budget for 1-k RAM

Circuits	Power
Bit decoder-drivers, 16 (standby)	87 mW
Word decoder-drivers, 16 (standby)	290
Sense amplifiers, 4	51
Write amplifiers, 4	137
Precharge-gate control driver	100
1-k cell array (standby)	5
	670 mW
Estimated (not simulated):	
Input inverters and I/O latches, 12 and 16	∿200
Timing and control	∿100
Total	∿1 W

SECTION 5

MEMORY TEST CHIP

A test chip was designed for the purpose of experimentally investigating the memory cell and subcircuit designs and exploring critical fabrication issues. A photomask set based on this chip design was procured and will be used to fabricate test chips during the second year of this memory study program.

A CAD plot of several levels of the mask set is shown in Figure 5-1. The chip, which measures 3.6 by 2.1 mm^2 (140 by 83 mil^2), contains the test devices and memory subcircuits listed in Table 5-1. The individual ENFETs and DFETs will be used for device characterization and for checking and improving device models. The FET gates are nominally 1-μm long, and the design values for the ENFET and DFET pinch-off voltages are +0.1 V and -1.0 V, respectively. The resistor patterns will be used to determine the minimum area in which the memory cell load resistors can be reliably fabricated. The loads in ENFET static RAM cells are expected to be on the order of 50 kΩ, and their physical size, if too large, would significantly increase cell area and layout. The primary purpose of the metal-dielectric-metal (MDM) capacitors is to simulate capacitive line loading during transient response measurements. The designs of the memory cells and subcircuits follow those described in Sections 2 and 3. The dc characteristics of these circuits will be measured and compared with the results of our design analyses and computer simulations. Each will be checked for functional performance and dc compatibility with the other subcircuits. Nearly all of the various circuit nodes are provided with probe pads to allow full dc characterization. Interconnection of the test circuits will be possible through the use of wire bonds. High-speed measurements will also be made to evaluate the transient response and power characteristics of the circuits. The test circuits are designed to simulate conditions appropriate to a 1-kbit RAM partitioned into four 256-bit (16 x 16) arrays: MDM capacitors are included to simulate line capacitances and extra FETs are used to simulate the capacitive loading of unaddressed cells and switched-off peripheral circuits. Master-slave flip flops, which substitute for I/O latches on the chip, have been included to assist in the measurement

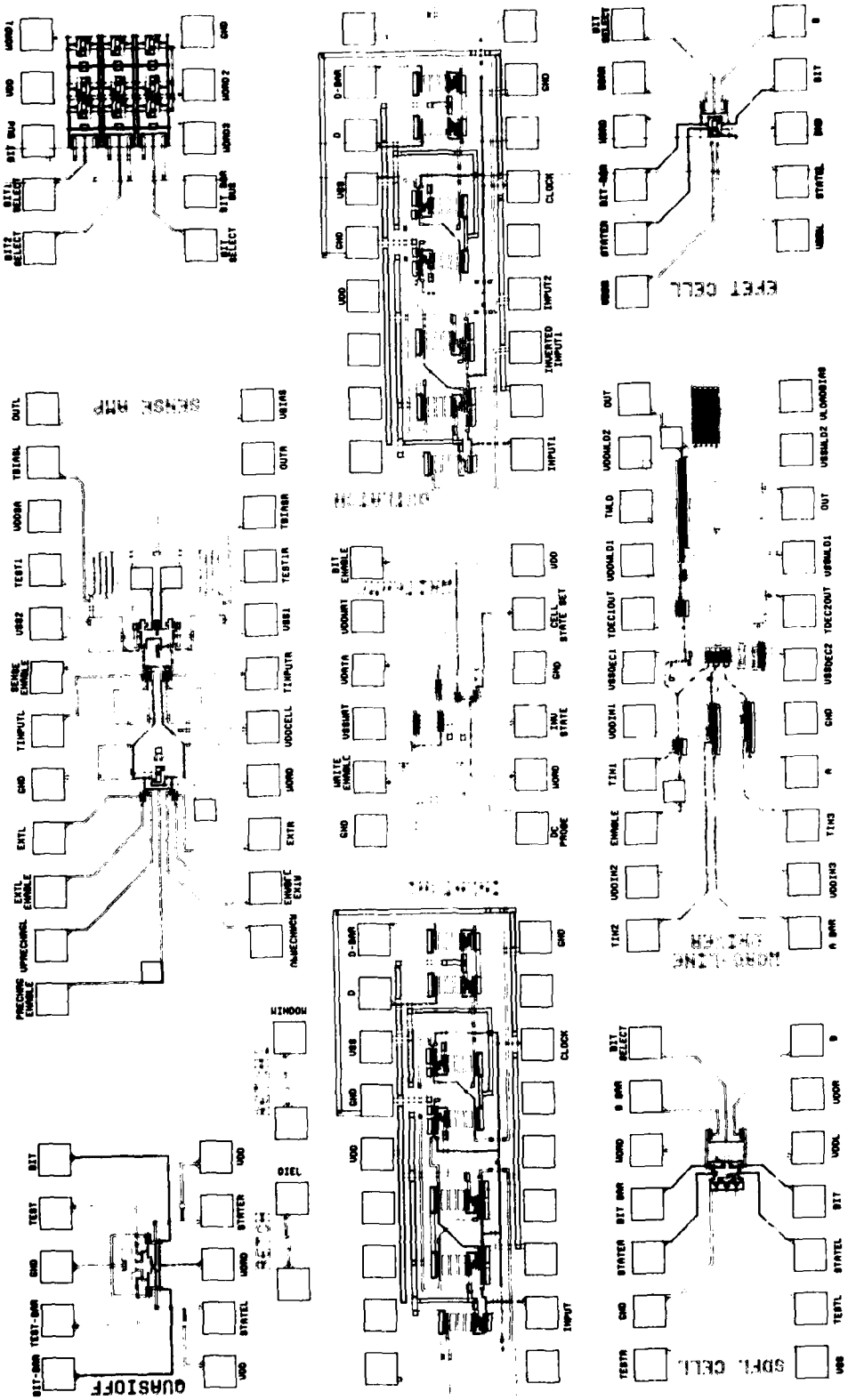


Figure 5-1. Layout of memory test chip.

Table 5-1. Test Chip Contents

Devices and components	ENFETs
	DFETs
	Schottky-barrier diodes
	Resistors (GaAs)
	Capacitors (metal-dielectric-metal)
Circuits	Static RAM memory cells
	ENFET cells (single and 3 x 3 array)
	Schottky-diode FET logic (SDFL) cell
	Quasi-normally-off cell
	RAM peripheral circuits
	Input and output flip flops
	Address decoder/word-line driver
	Write amplifier/driver
	Sense amplifier

of transient characteristics; i.e., they can be used to store desired input conditions and capture instantaneous transient response levels.

Descriptions of the major test circuits are given in the following paragraphs.

A. ENFET MEMORY CELLS

The schematic of the single ENFET memory cell is shown in Figure 5-2. The circuit includes the ENFET flip flop, the DFET word-address gates, and the bit-line select gates. This circuit will allow full dc characterization of the read, write, and standby operating modes. The actual circuit layout

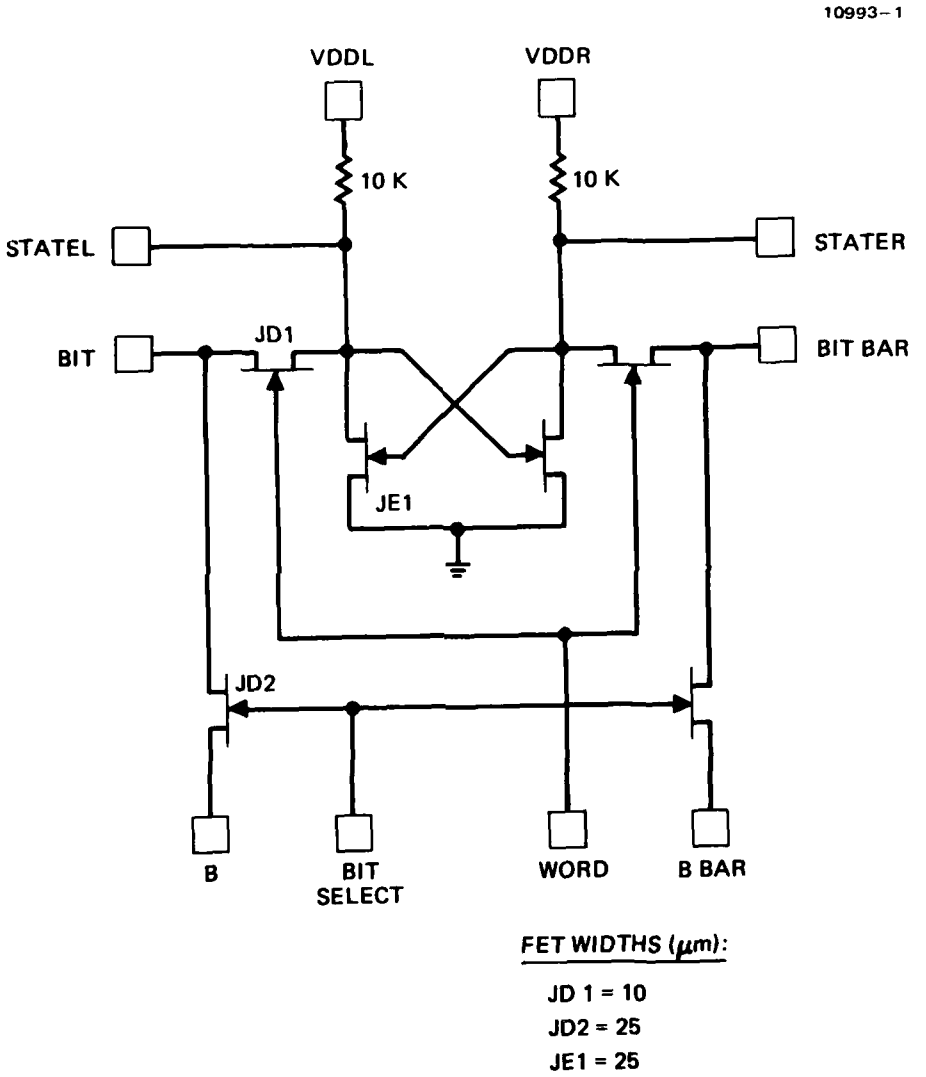


Figure 5-2. Schematic of the ENFET memory-cell test circuit. The JEs are ENFETs and the JDs are DFETs.

is shown in Figure 5-3 and corresponds closely with the preliminary layout shown earlier in Figure 2-3. The on-chip load resistors will initially be fabricated with n-type GaAs. Since it is difficult to achieve controlled n-type sheet resistivities above ∿1000 Ω per square by implantation, the test-chip loads are designed to be 10 kΩ, which is only one-fifth of the 50-kΩ design value. Off-chip resistors will be used to achieve the design value. This approach allows the cell size to approximate that of Figure 2-3. Later, when compact, higher resistivity loads are developed, the full 50-kΩ loads will be fabricated on chip.

The layout of the 3 x 3 ENFET cell array is shown in Figure 5-4. It incorporates nine of the single cells, plus the appropriate number of word lines, bit-lines, and bit-select FETs. Initially, the array cells will be restricted to the 10-kΩ load resistors since no provision is made for incorporating off-chip resistors in the cell circuits. The array test circuit will be used to investigate read, write, and standby operation as well as the effects of processing nonuniformities or possible intercell cross-talk.

B. ALTERNATIVE MEMORY CELLS

As possible alternatives to the ENFET memory cell, the test chip includes flip-flop memory cells based on the use of Schottky-diode FET logic (SDFL) inverters and quasi-normally-off (QNO), or quasi-ENFET, inverters. The schematic of the SDFL cell is shown in Figure 5-5. It incorporates all DFETs. Figure 5-6 shows the schematic of the QNO cell. It incorporates Type-3I inverters,[2] which are similar to SDFL inverters, except for the use of quasi-ENFETs (i.e., $-0.4\ V \leq V_p \leq 0.2\ V$) and the use of resistors in place of pull-down and pull-up FETs.

C. WRITE AMPLIFIER CIRCUIT

Figure 5-7 shows the schematic of the test circuit for the write amplifier, or write driver. The driver circuit corresponds to that shown in Figure 2-9. In addition to the amplifier, the test circuit includes a simulated bit line and one side of an ENFET memory cell. In addition to dc characterization of the write amplifier, this test circuit will be used to

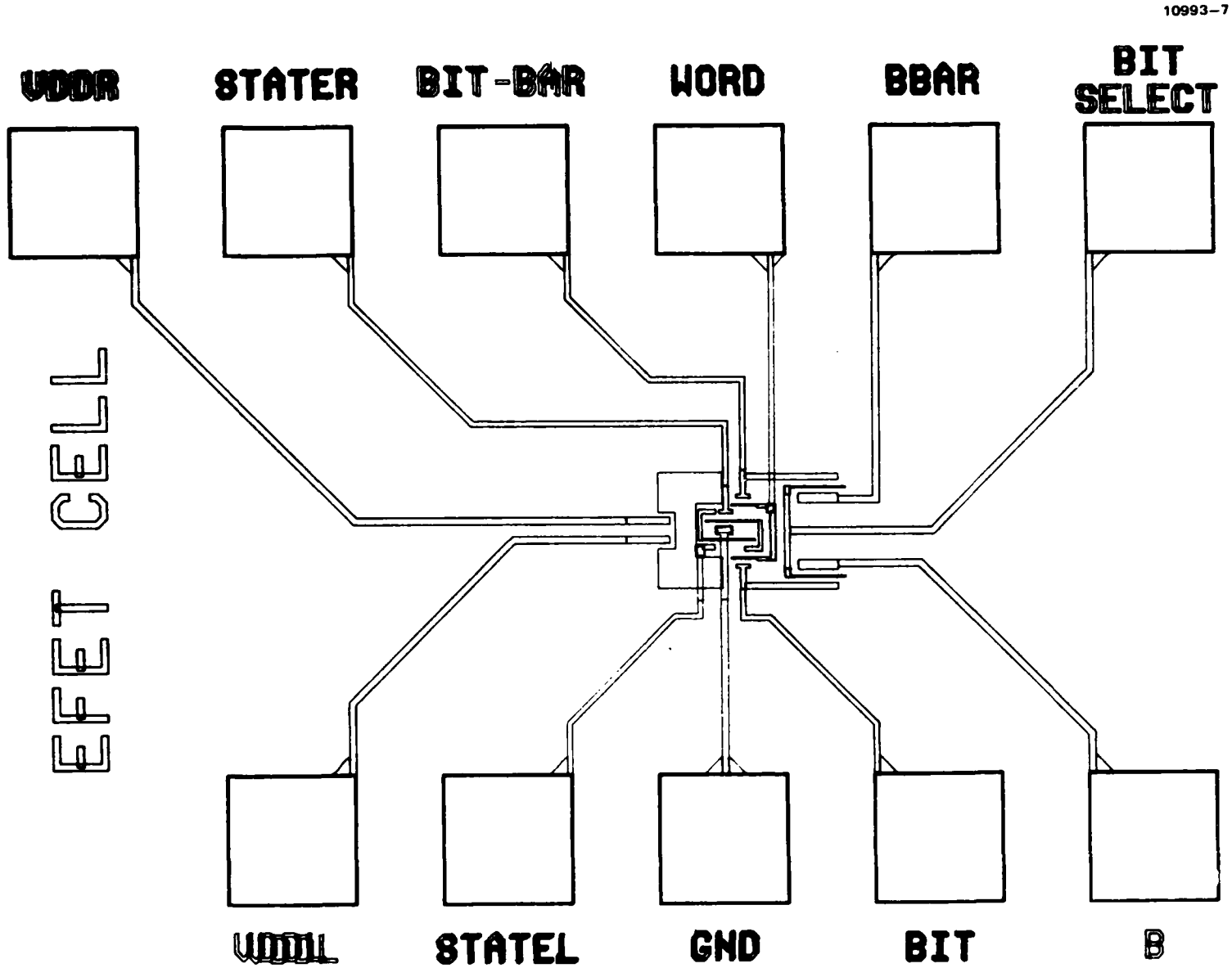


Figure 5-3. Layout of the ENFET memory cell. The probe pads are 75-μm square.

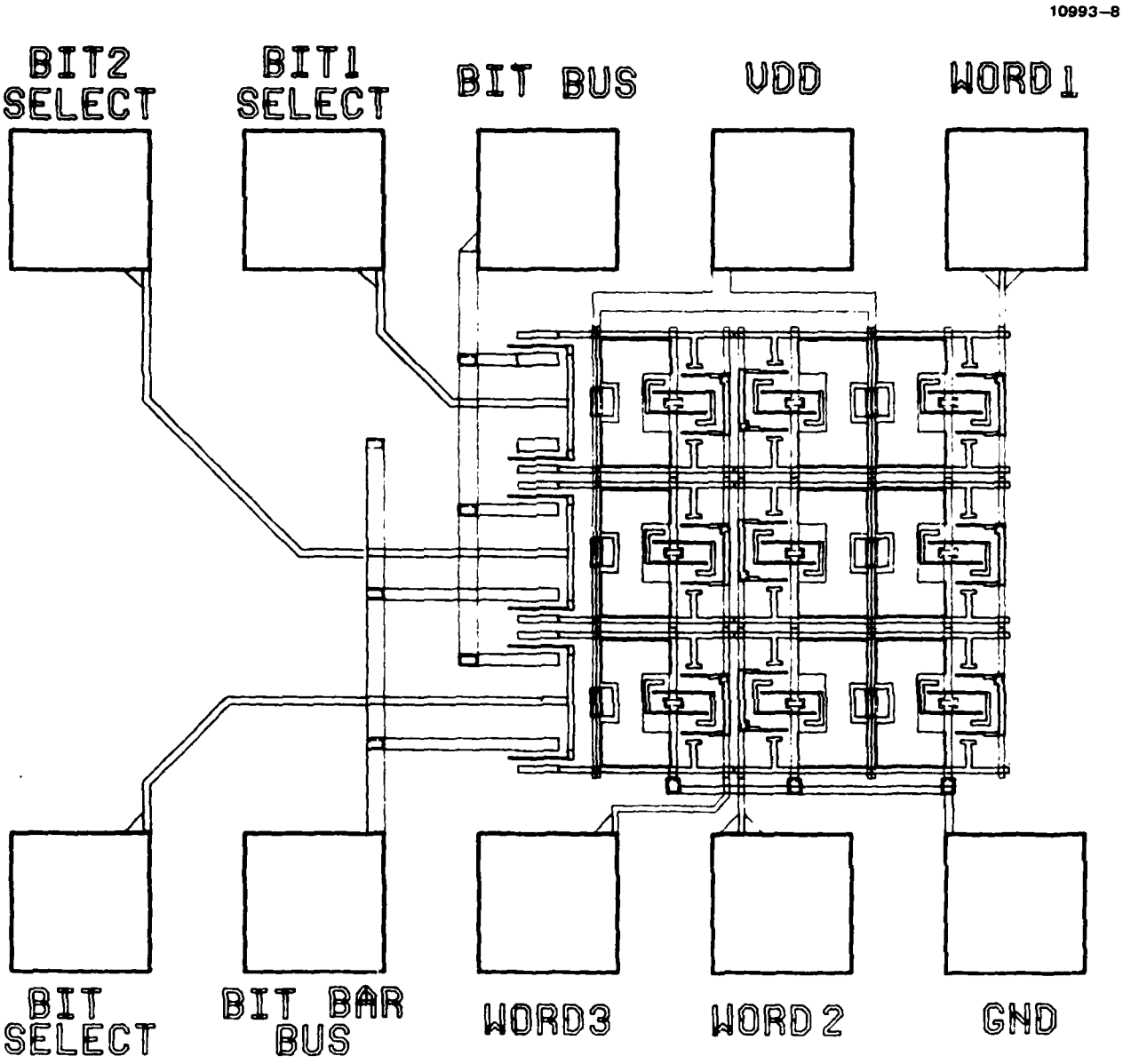


Figure 5-4. Layout of the 3 x 3 ENFET cell array.

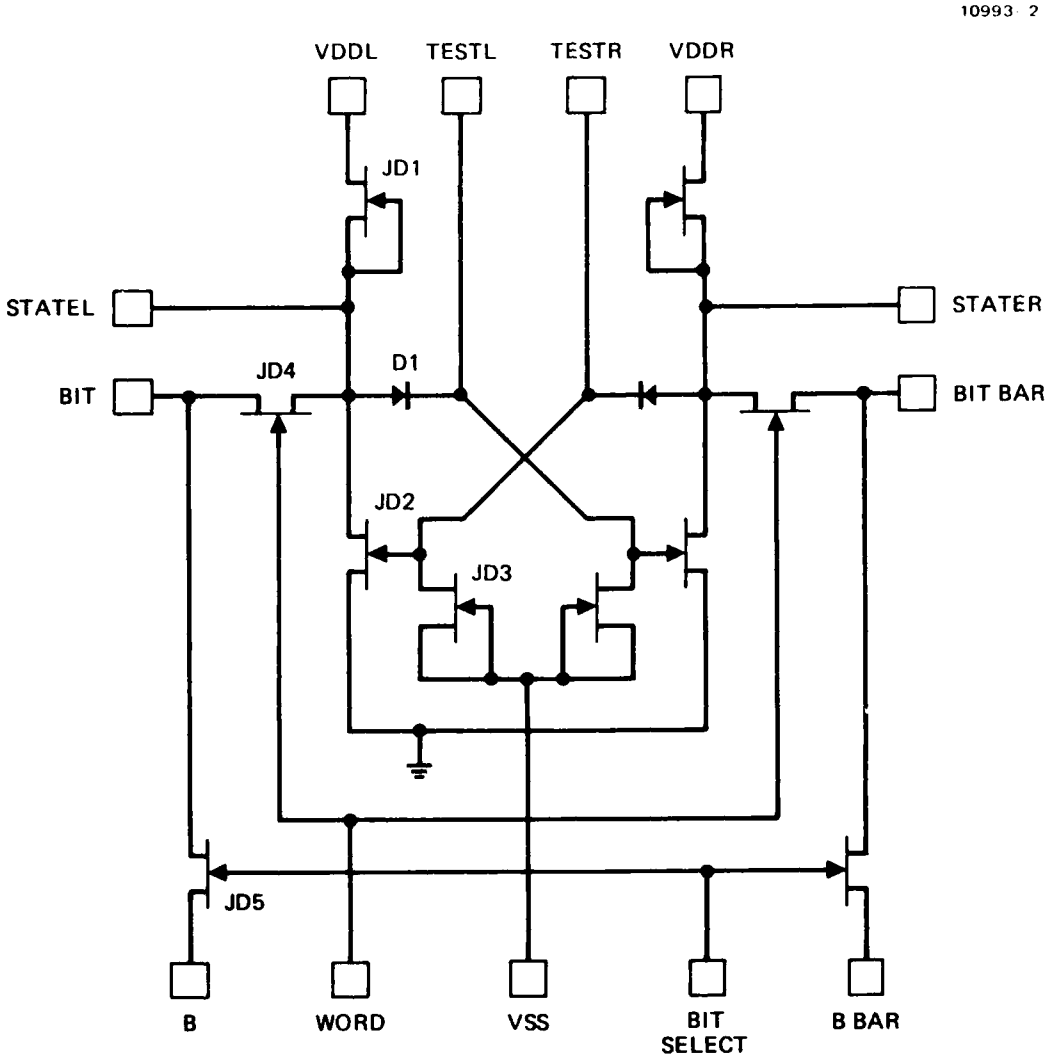


Figure 5-5. Schematic of SDFL memory-cell test circuit.

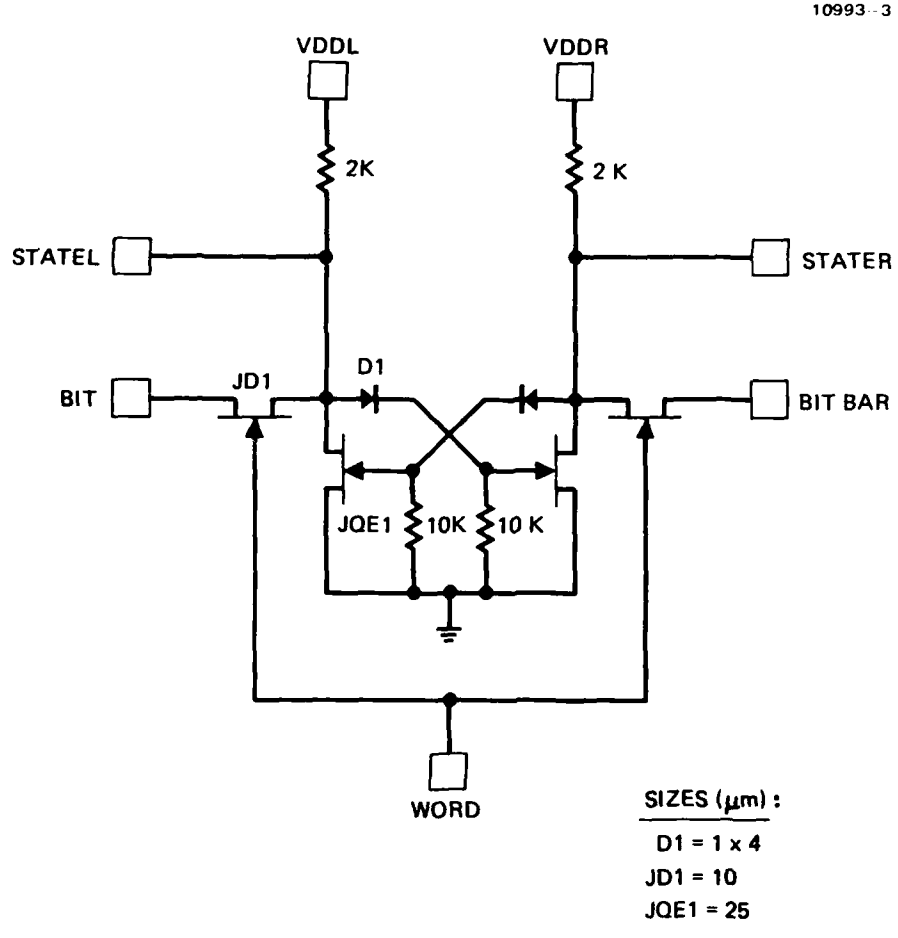


Figure 5-6. Schematic of QNO memory-cell test circuit. JQE1 is a quasi-ENFET.

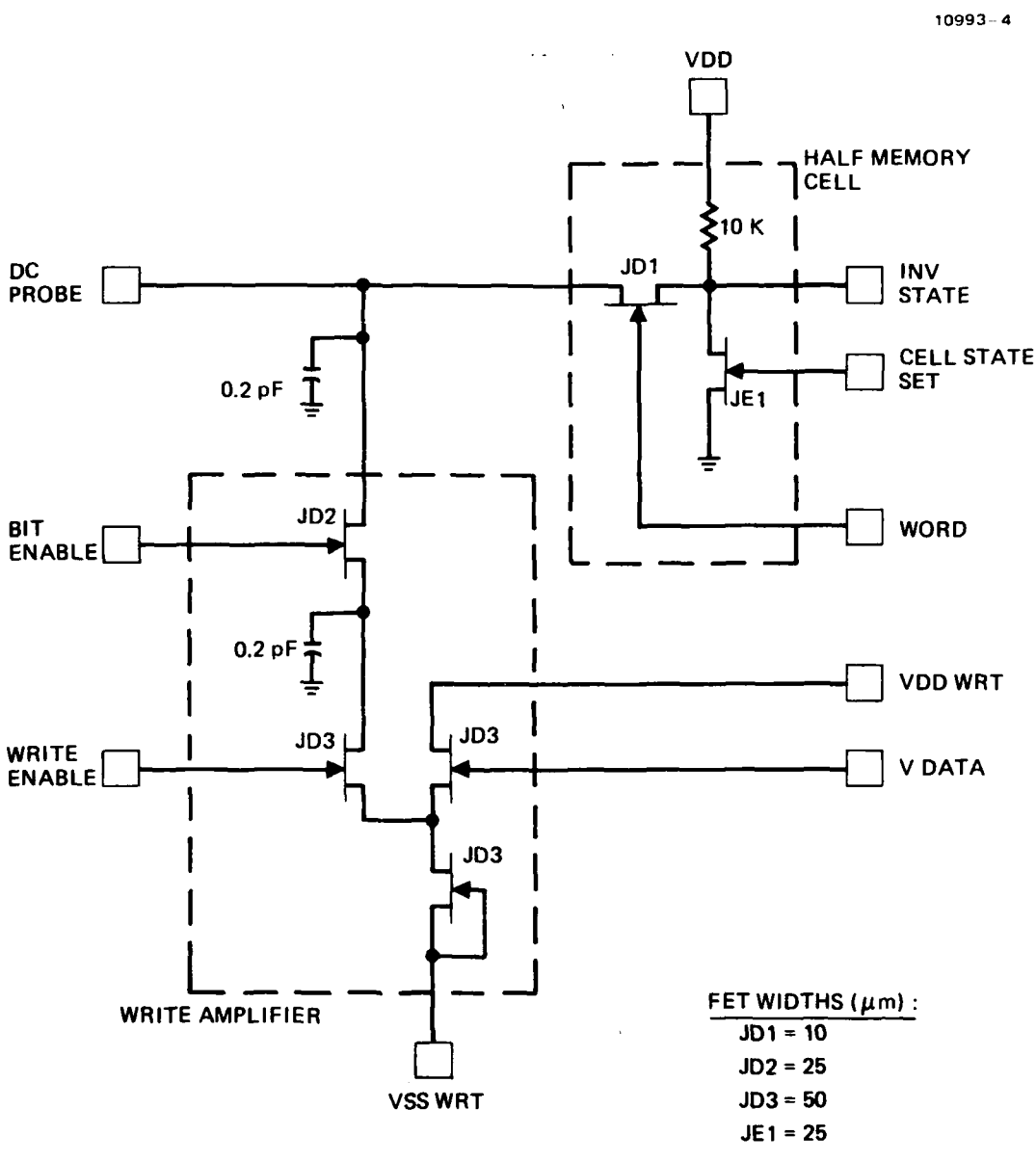


Figure 5-7. Schematic of write-amplifier test circuit driving a simulated bit line and one side of an ENFET memory cell.

investigate the bit-line response time during the write mode. Figure 5-8 shows the layout of this test circuit.

D. ADDRESS DECODER AND WORD-LINE DRIVER

Address decoders and line drivers are needed in a RAM for selecting and driving both the word lines and the bit lines corresponding to the addressed memory cell. Our analysis shows that the word-line driver presents the larger load requirement; therefore it was selected for inclusion on the memory test chip. It will be used for dc design confirmation and to determine the word-line response time during cell select. The schematic for the test circuit is shown in Figure 5-9. It corresponds to the circuit of Figure 3-3; however, the design of the test circuit has been modified to simulate the dc and transient loading of a 1-kbit memory. In addition, the inputs to the test circuit include inverters that serve to buffer the inputs and provide level shifting necessary to bring the input signals up to SDFL logic levels; these inverters would normally be part of the input latches. The layout for the address decoder and word-line driver is shown in Figure 5-10.

E. ENFET CELL AND SENSE AMPLIFIER

To test the dc characteristics of the sense-amplifier design and measure the read-mode response time, the test chip includes the circuit shown in Figure 5-11. It contains both an ENFET memory cell and a sense amplifier (Figure 2-7). Either circuit can be tested individually, or the combination can be used to measure the dc and transient characteristics of the read mode, including the capacitive loading effects of the bit lines. Finally, the layout of the test circuit is shown in Figure 5-12.

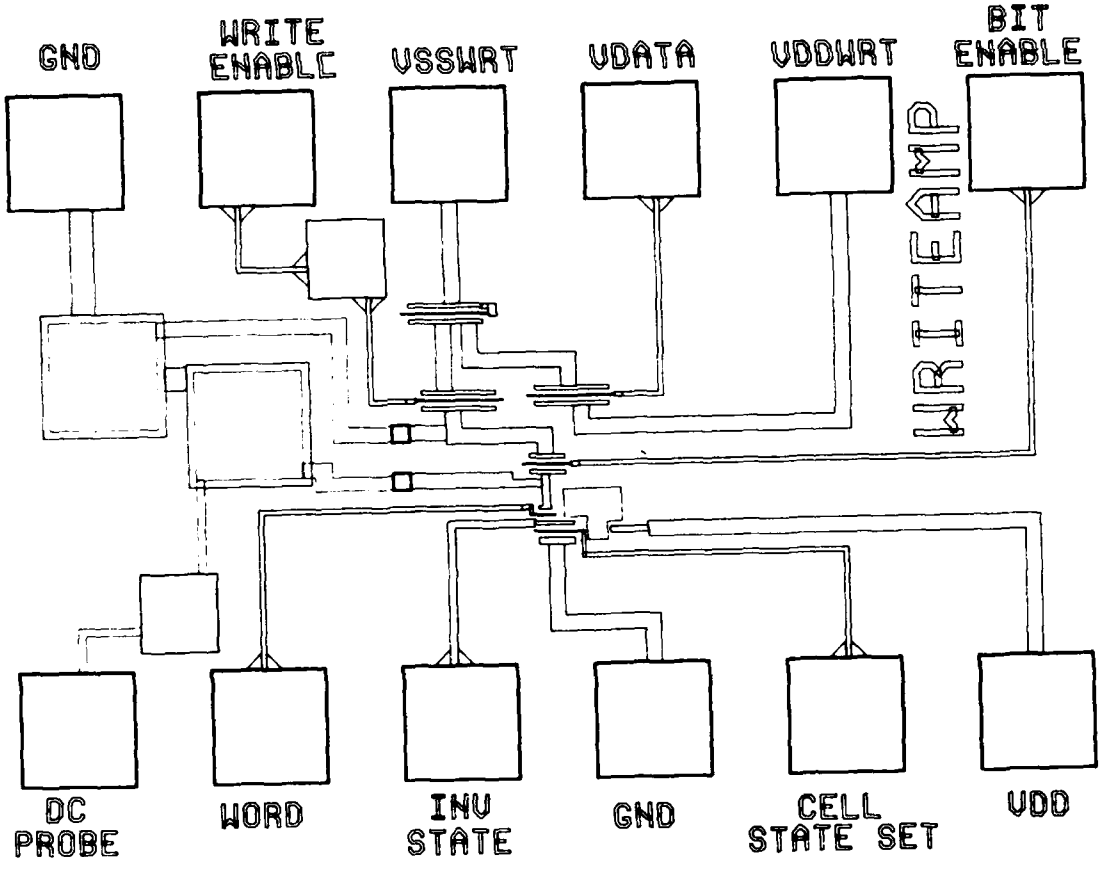


Figure 5-8. Layout of write-amplifier test circuit.

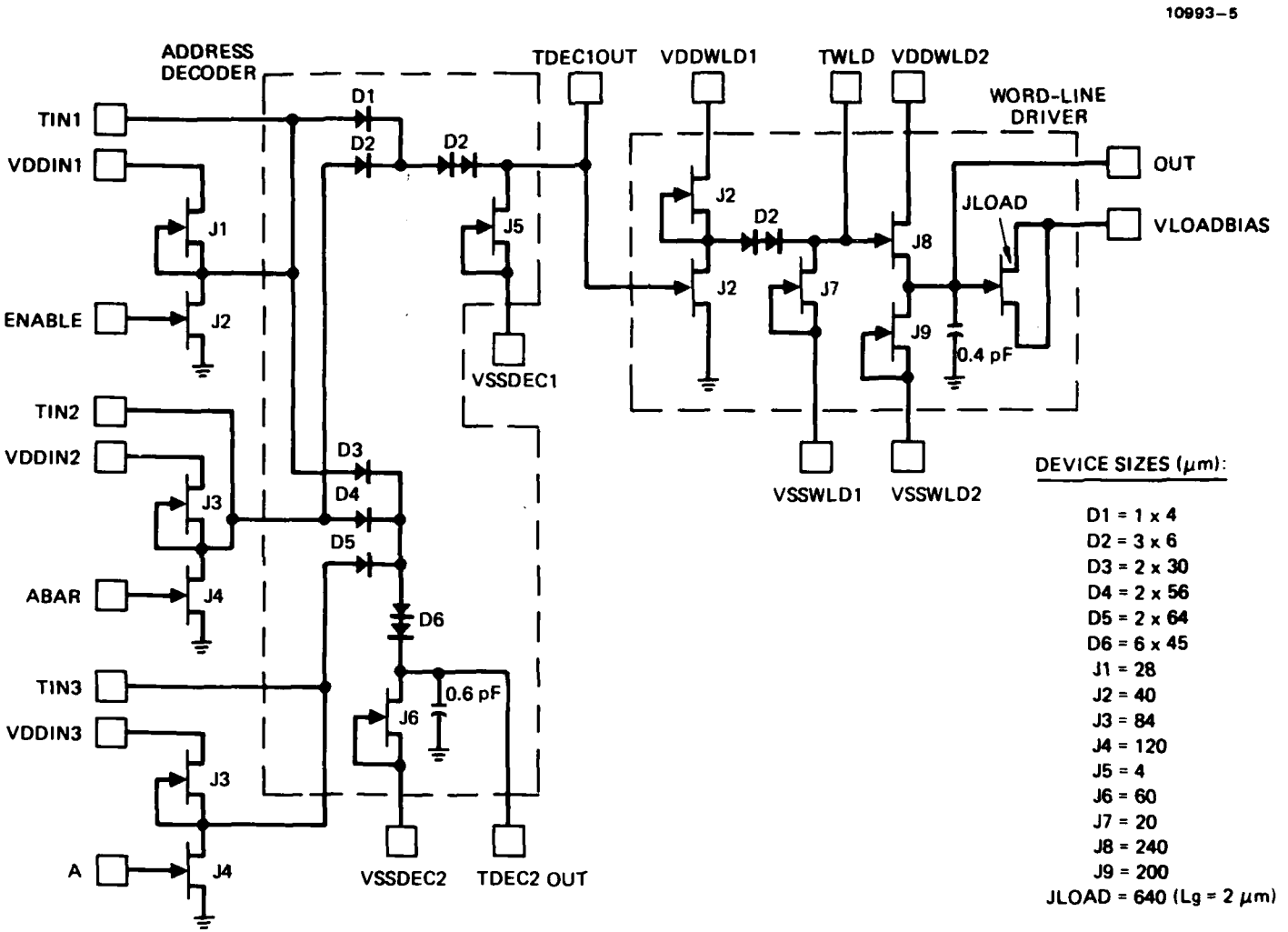


Figure 5-9. Schematic of the test circuit for an address decoder and word-line driver.

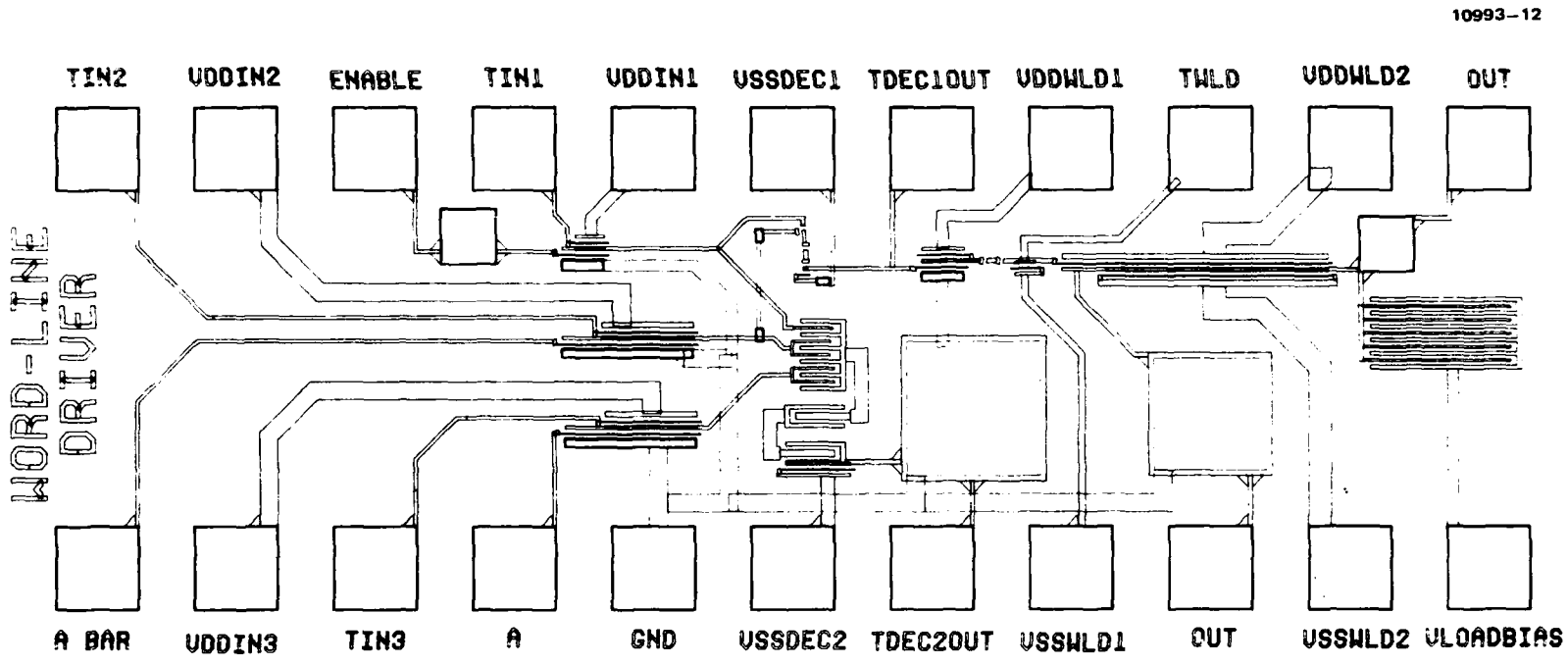


Figure 5-10. Layout of address decoder and word-line driver test circuit.

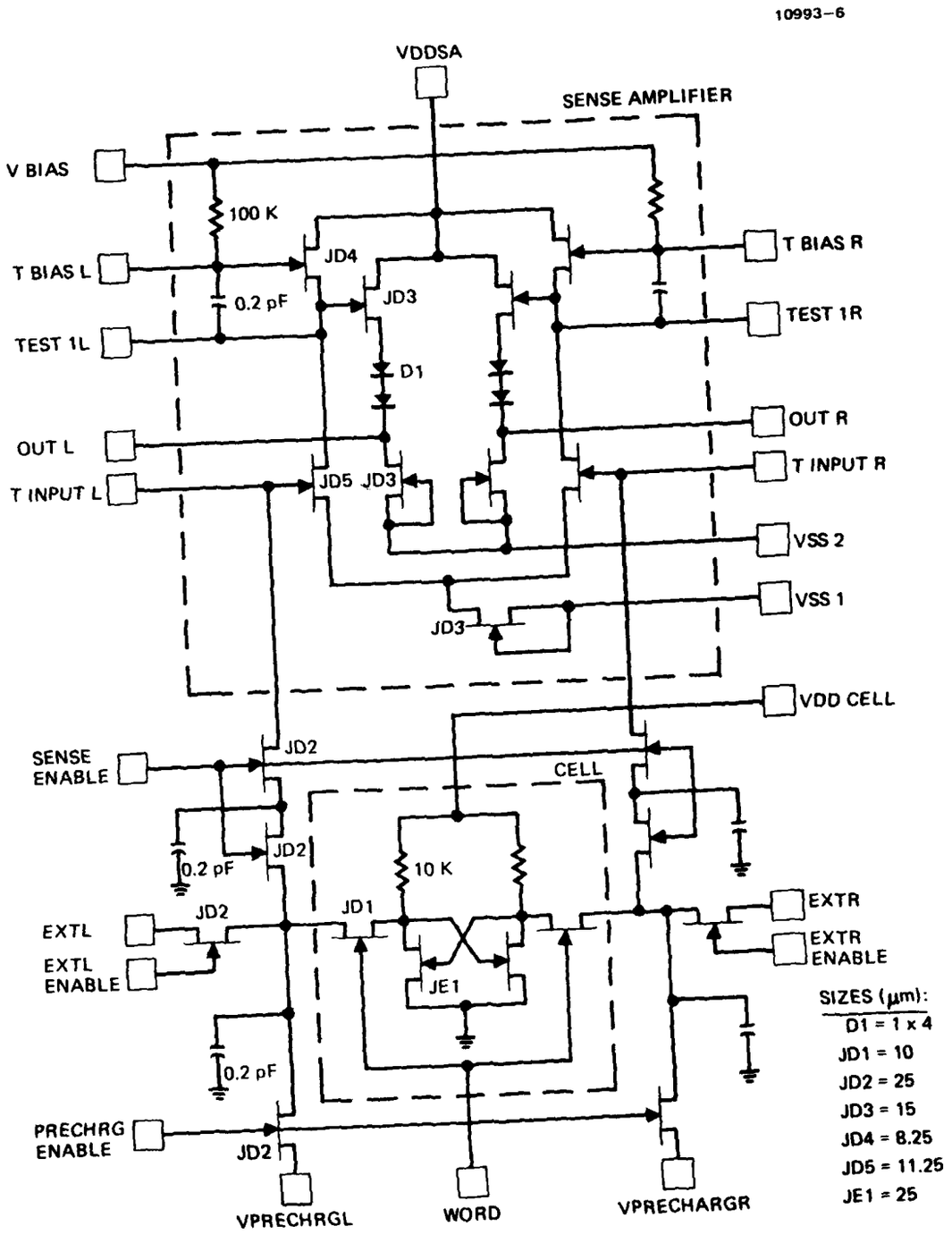


Figure 5-11. Test circuit containing both an ENFET cell and a sense amplifier.

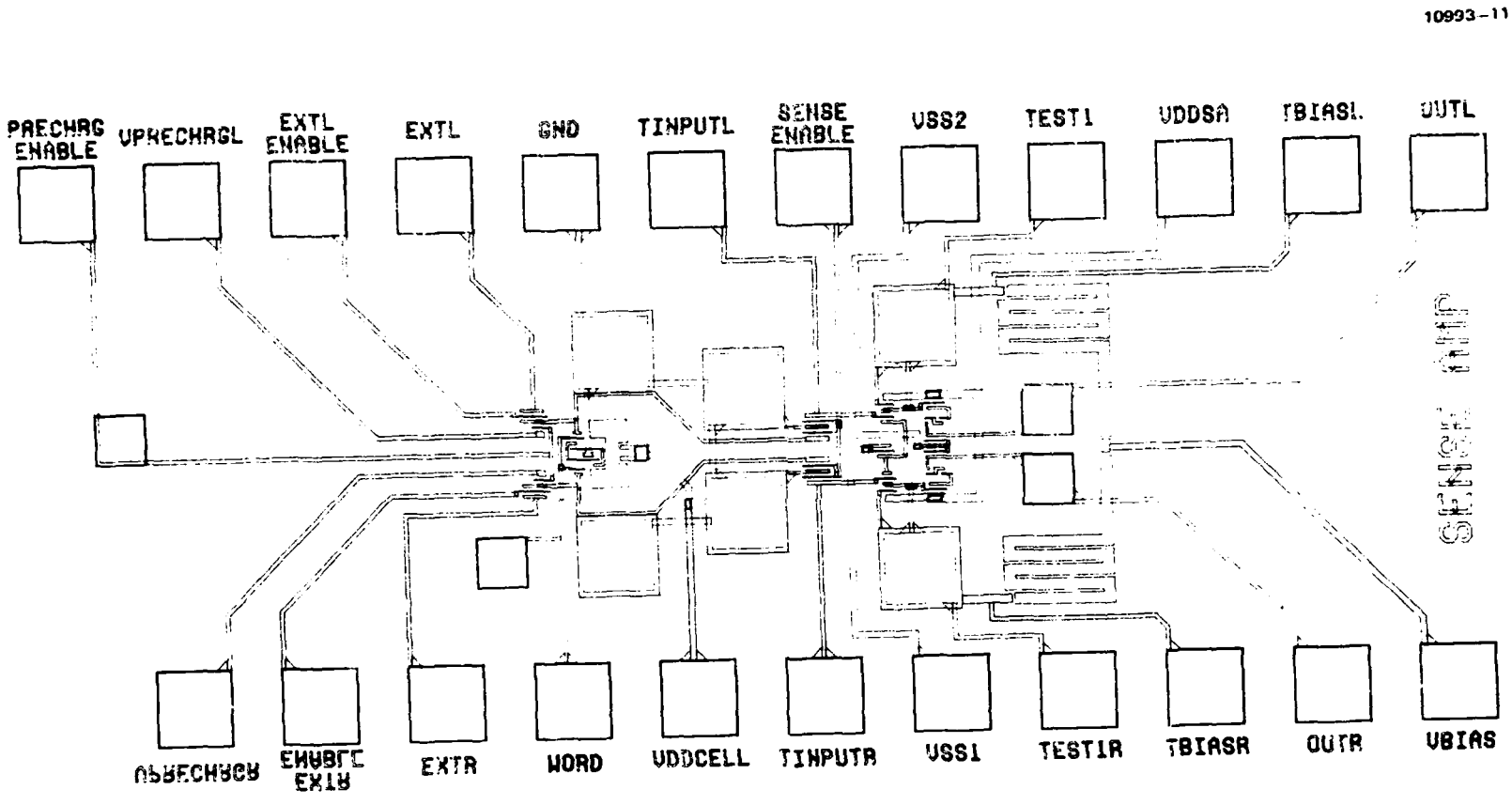


Figure 5-12. Layout of the ENFET cell-sense amplifier test circuit.

SECTION 6

CONCLUSIONS

An initial design and analysis study of potential high-speed GaAs memory circuits was performed. The results show that a 1-kbit static RAM having a 1-nsec access time and 1-W dissipation is achievable. The memory cell design uses low-power ENFET inverters to implement a static set-reset flip flop. Access to each cell is controlled by DFET switches. The calculated power dissipation is only 5 μW per cell. To achieve maximum memory speed, the peripheral memory control and drive circuitry was designed with DFETs exclusively. These peripheral circuits will account for nearly all of the power dissipated by the memory, and close attention must be given to their design, especially the line-driver circuits. SPICE2 simulations were used to estimate the read and write transient-response times of the several memory subcircuits. These analyses included the effects of parasitic and interconnect line capacitances appropriate for a 1-kbit array. The total sum of the predicted response times is slightly greater than 1 nsec, but optimum operational sequencing will provide some overlap of the various functions and allow for 1-nsec access. The detailed operational sequencing is still to be developed, however.

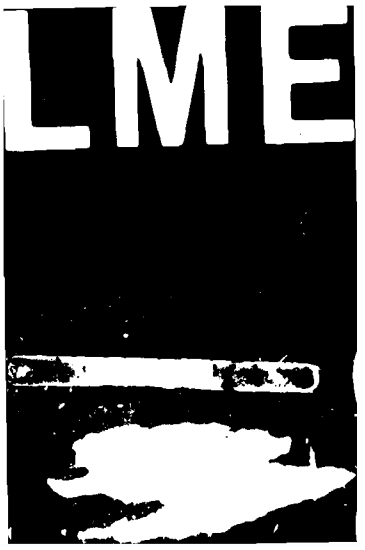
Experimental testing and characterization of the proposed circuit designs are now required. A memory test chip was designed for this purpose, and during the second year of the program, this test chip will be fabricated and used to measure the dc and transient characteristics of the major memory circuits. It will also be used to investigate some fundamental technological issues such as: the relationship between substrate materials, fabrication processes, and resulting device parameter uniformity; practical means for fabricating compact, high-resistance ($\geq$50 kΩ) load resistors; and potential isolation problems associated with the high packing densities required for area-efficient memory-cell arrays.

REFERENCES

1. R.C. Eden, B.M. Welch, and R. Zucca, "Low Power GaAs Digital ICs Using Schottky Diode-FET Logic," Digest of Technical Papers, 1978 International Solid-State Circuits Conference, 68-69 (February 1978).

2. G. Nuzillat, G. Bert, T.P. Ngu, and M. Gloanee, "Quasi-Normally-Off MESFET Logic for High-Performance GaAs ICs," IEEE Trans. Electron Devices ED-27, 1102-1109 (June 1980).

3. R.L. Van Tuyl and C.A. Liechti, "High-Speed Integrated Logic with GaAs MESFETs," IEEE J. Solid-State Circuits SC-9, 269-276 (October 1974).


LME